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Structures for High Frequency Transistor

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This report is presented in two parts. Part I studies submicron vertical-flow field transistors, with Schottky gates, to see if ballistic electron injection could yield improved results for future high frequency transistors. Part II studies layer stability and contact formation in GaAs structures.

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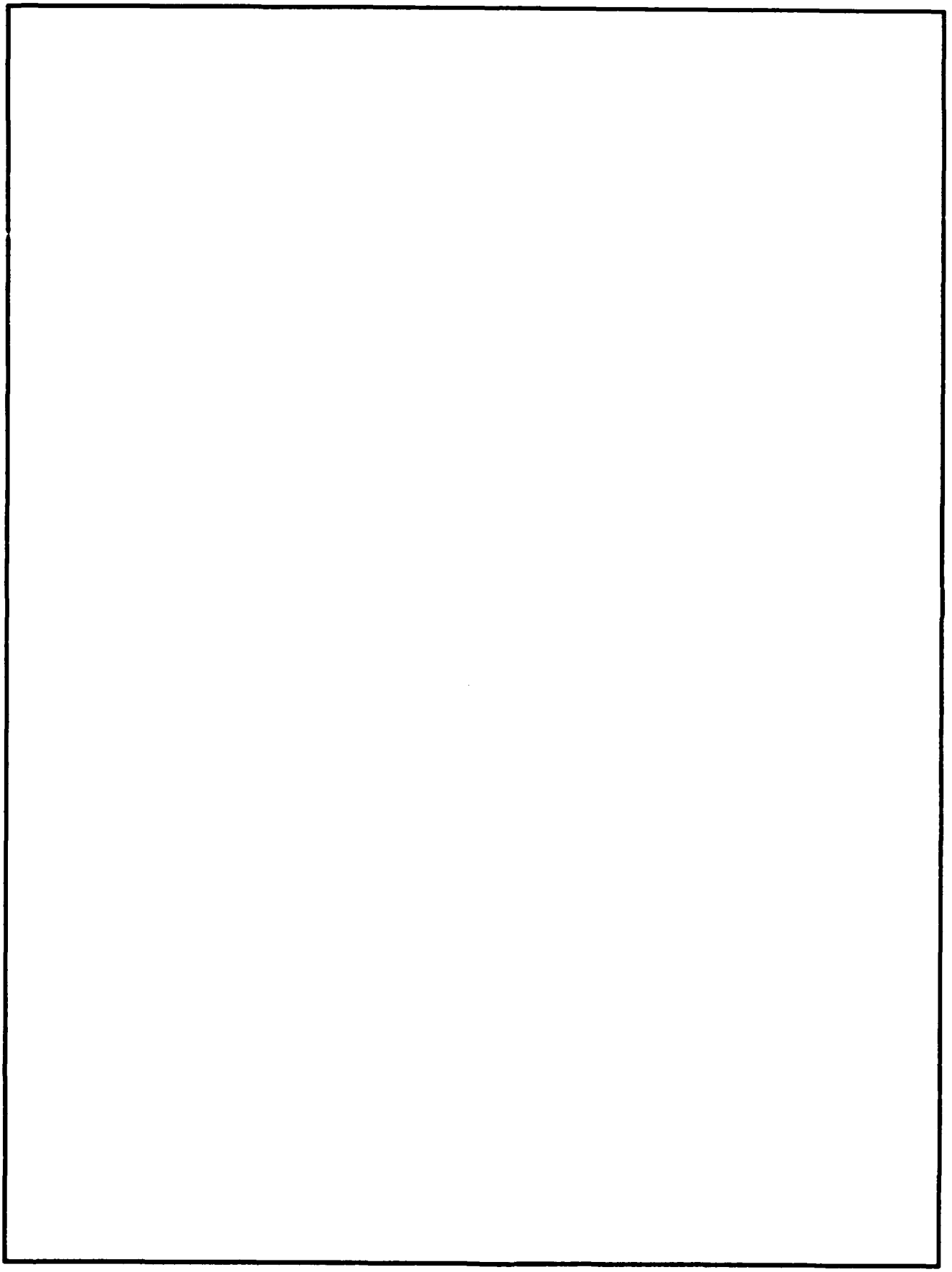

ABSTRACT

Part I: Submicron vertical electron flow structures were grown by molecular beam epitaxy (MBE) with and without ballistic electron launchers. Both electron flow down toward the substrate and up away from the substrate were studied. Angle evaporation of metal, on the sides of etched vertical channels, was used to form Schottky gates. The placement of the gates at the launch plane for ballistic electrons was found to be critical. The case with electrons flowing down had .5 μm drift space for the electrons and 2 x $10^{16}/cm^3$ doping and yielded low g_m values ≤ 50 mS/mm. With high source resistance, high electron injection energy and .5 μm drift space, these devices generally performed poorly. Those with ballistic electron injection worked more poorly than those without. The case with electrons flowing up had .13 μm drift and 1 x $10^{17}/cm^3$ doping and yielded higher g_m values of 160 and 240 mS/mm at 300 and 77°K, respectively. The electron velocity values in the latter case for electrons flowing up were about 3 and about 6 x 10^7cm/s without and with ballistic electron launchers. The devices with electron flowing up were to short (.13 μm) and too thick between opposing Schottky gates (.6 μm) to allow device current cut off. The results, however, do show high promise for such vertical FET's with ballistic electron injection.

Part II: Ohmic contacts with improved performance and stability on n-type GaAs were studied using poly-Si on GaAs, Co on GaAs, and epitaxial Ge on GaAs. The poly-Si on GaAs yielded $10^{-4}\Omega\text{-cm}^2$ when 9% As doped and annealed at $1000^{o}C$ The Co on GaAs formed a solid phase with GaAs at $500^{o}C$. Epitaxial Ge on GaAs was formed by solid phase epitaxy on clean surfaces after 400°C annealing of the deposited amorphous Ge. The contact was ohmic, but had high specific contact resistance.

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I.A. PROGRAM OBJECTIVE FOR PART I

The objective for Part I was to study submicron vertical-flow field effect transistors, with Schottky gates, to see if ballistic electron injection could yield improved results for future high frequency transistors. Instead of average transit velocity values in the range of 1-2x10^7 cm/s, or even 3-5x10^7 cm/s as in very short accelerating drift region, values in the range of 6-8x10^7 cm/s were sought. Such ballistic electron launchers, when optimized, could then be put in optimized vertical transistors, such as permeable base transistors, to sharply raise the unity current gain frequency from its present PBT value of only 40 GHz to values at above 100 GHz.

I.B. TECHNICAL PROBLEM FOR PART I

There were several key problems in optimizing the performance of submicron, vertical electron flow, Schottky-gated field effect transistors with ballistic electron injection. The most important one was optimizing the ballistic electron launch energy and the electron drift region to obtain high average electorn velocity during the electron transit through the device. The technological problems associated with the device fabrication involved the achievement of thin vertical channels that could be pinched off with ~.1μm Schottky gates on both sides. In addition, reaching the high performance expected meant obtaining very low source contact

resistance when the top of the channels were used as the source.

I.C. SUMMARY FOR PART I

In the work of this project, GaAs vertical field-effect transistors of fully submicron dimensions were first fabricated with source up and with both launcherless, MESFET design and with n^+-n^--n^+ design, incorporating four different types of hot-electron injection cathodes. The four thermionic emission injection structures studied were the heterojunction, graded heterojunction, and heterojunction dipole launchers, all in AlGaAs/GaAs, and the homojunction planar-doped barrier launcher. Measured zero bias barrier heights were in the range 0.084 to 0.27 eV and compared favorably with values from theoretical conduction band simulations. Measured saturation current densities were in the range 4.4 to 29.0 kA/cm^2, well below the desired value of $\sim 10^5 A/cm^2$. For comparison, the launcherless MESFET ($n_{ch} = 2 \times 10^{17} cm^{-3}$) fabricated for comparison exhibited a current density greater than $3 \times 10^5 A/cm^2$. The fundamental limit to the saturation current density of the launcher-containing structures studied in this work is attributed to the combination of the light channel doping of $2 \times 10^{16} cm^{-3}$ and the failure to achieve the desired enhanced average electron velocity of $\sim 4 \times 10^7 cm/sec$. For an average electron velocity in the channel of $v_{sat} = 1.2 \times 10^7 cm/sec$, for example, the channel can only be expected to support a current density of 38 kA/cm^2, which is of the same order of magnitude as the best measured value of 29 kA/cm^2 for the PDB with gate-on-launcher. Further discussion of the limitations of the launcher-channel

structures studied and suggestions for the degree of future launcher structures will be presented later.

Reproducible, high-yield process technology for the conventional (fully undercut) cross section device structure was developed utilizing mid-UV optical contact lithography, Ar ion milling, and wet chemical etching. The devices fabricated typically had 0.6 μm-wide source fingers on a 2 μm period, 0.3-0.4 μm-wide channels, 0.5 μm source-drain spacings, and ≤ 0.25 μm gate lengths, the latter by angled shadow evaporation. An alternate device structure for the heterojunction-containing devices, known as the wide-source cross section, was investigated and was shown to allow selective angle, self-aligned gate deposition, providing a significant reduction in gate capacitance and ~100 nm gate-source spacings. The wide-source cross section would require additional development to increase yield and is not applicable to homojunction structures.

The intent of the inclusion of the electron launcher structures was to increase the average electron velocity through the active channel, thereby improving the device transconductance and the potential for high frequency operation. The results of the DC characterization of the launcher-containing device structures of this work, however, revealed a degradation in device performance compared to that of either the vertical MESFET of this work or the launcherless vertical FET ($n_{ch} = 5 \times 10^{16} cm^{-3}$) of [4]. Measured extrinsic transconductances were in the range 11 to 28 mS/mm for the launcher-containing devices compared to 52 and 51 mS/mm for the vertical MESFET of this work and the launcherless vertical FET

of Mishra, respectively, adjusted for differences in channel doping. Based on the disappointing performance of devices with gate placement below the launcher and motivated by the possibility of directly modulating the injection process, an investigation was made of the effects of gate placement relative to the launcher in PDB-containing device structures. Rather than resulting in improved intrinsic device performance, increasing gate-launcher overlap was seen to improve extrinsic device performance (to 34 mS/mm) due to the reduction of the effective source resistance.

Comparison of the DC parameters for the launcher-containing devices with those for the vertical MESFET of this work reveal the two primary problems of the launcher-containing devices studied in this work. These are an increased effective source resistance and a decreased saturation current density, both of which result in decreased extrinsic transconductance and both of which must be attributed to the launcher-channel structures present in these devices but not in the vertical MESFET.

Consider, first, the issue of source resistance. The source resistance in the vertical MESFET is dominated by the ohmic contact resistance. The specific source resistance measured for the vertical MESFET of this was 1.6 x 10-6Ω-cm^2 which is a good number for a AuGe-based contact to n$^+$-GaAs. The relatively small active area-to-gate periphery ratio of the device structure used in this work, however, results in a normalized source resistance value of 0.9 Ω-mm, a value which is almost an order of magnitude higher than for typical results for planar MESFET's and MODFET's, although

not so high as to rule out adequate device performance. The use of an overgrown structure as in the Permeable Base Transistor (PBT) [5-6] could be used to alleviate the low active area-to-gate periphery ratio problem in the device structures of this work.

The source resistance in the launcher-containing structures, on the other hand, consists of three components, the ohmic contact resistance, the launcher series resistance, and the parasitic channel series resistance. The ohmic contact resistance should be the same as that for the vertical MESFET. The launcher series resistance was estimated to be ~ 2.5 x $10^{-6}\Omega$-cm^2, assuming a current density of $10^5 A/cm^2$ at a launcher bias of 0.25 V. The value of the launcher series resistance could be much higher for smaller current densities at the same launcher bias. Finally, the parasitic channel series resistance can be calculated to be ~ 0.8 x $10^{-6}\Omega$-cm^2 for a 0.1 μm-long, 0.3 μm-wide parasitic channel doped at 2 x $10^{16} cm^{-3}$ and depleted 0.1 μm on each side. On the basis of these approximate calculations, one would expect the launcher-containing devices to exhibit source resistances at least a factor of three higher than those of the vertical MESFET. In fact, the measured normalized source resistances were in the range 2.9 to 25 Ω-mm, the average value being about 7.5 Ω-mm. These values must be reduced for device performance to approach desired levels. The ohmic contact resistance may be reduced by using a sintered Ti/Pt/Au contact to a graded n^+-InGaAs source capping layer. Using this technique, Nagata et al. [7] have achieved a specific contact resistance of 1.4 x $10^{-7}\Omega$-cm^2, an order of magnitude below the value for the alloyed

AuGe-based contact used in this work. Reduction of the launcher series resistance will occur concurrently with the increase in device current density which is a function of the design of the launcher-channel structure to be discussed subsequently. It has already been shown that the parasitic channel series resistance is reduced by depositing the gate astride the launcher. In the PDB launcher structures studied, the overall specific source resistance was reduced by more than a factor of four, from 40 x $10^{-6}\Omega$-cm^2 for the gate 800 Å below the launcher, to 8.9 x $10^{-6}\Omega$-cm^2 for the gate overlapping the launcher by 1670 Å. Alternate methods to reduce the parasitic channel series resistance would be to increase the channel doping or use an overgrown device structure as in the PBT which would eliminate detrimental surface depletion effects.

Now consider the issue of current density. Having attributed the reduction in device current density, with its attendant reduction in device transconductance, in the launcher-containing devices, compared to the vertical MESFET and launcherless vertical FET of Mishra, to the launcher-channel structures studied, one must examine the design and operation of the launcher-channel structures in detail. During the course of this work, launcher development was pursued primarily by investigating different types of launchers (e.g., heterojunctions, PDB) while maintaining a fixed launcher/channel doping ratio of fifteen (ten for the PDB devices). This launcher/channel doping ratio had been determined from an empirical treatment of current continuity in the launcher-channel structure assuming an enhanced electron velocity in the channel,

immediately downstream from the launcher, of ~ 6 x 10^7cm/sec. Failure to achieve this enhanced velocity in the lightly-doped channel, in practice, results in the device current density being limited by the electron transport in the channel and not by the launcher itself. Put differently, the launcher does not (and cannot) achieve the flat band bias condition as desired for maximum current and injection energy. A further clarification of the launcher/channel doping ratio required for flat band operation of an AlGaAs/GaAs heterojunction launcher structure has been recently provided by Al-Omar et al. [8]. There presents a simple physical criterion for achieving flatband,

$$n_d(Al_xGa_{1-x})\, v_{th}(x,T) \leq n_d(GaAs)\, v_{ch}^{eff}$$

where $n_d(Al_xGa_{1-x}As)$ and $n_d(GaAs)$ are the doping levels in the AlGaAs launcher and GaAs channel, respectively, $v_{th}(x,T)$ is the Al-mole fraction and temperature dependent thermal velocity in the AlGaAs, and v_{ch}^{eff} is the effective electron velocity in the GaAs channel. Substituting appropriate room temperature values for the heterojunction launcher-channel structure of this work and taking a value of 4 x 10^7cm/sec for v_{ch}^{eff}, one sees that the inequality of the equation is not satisfied:

$$(3 \times 10^{17}cm^{-3})(6 \times 10^6cm/sec \leq (2 \times 10^{16}cm^{-3})(4 \times 10^7cm/sec)$$

The inequality would be satisfied for a channel doping of 6 x $10^{16}cm^{-3}$, for example, provided that an effective electron velocity

of 4 x 10^7cm/sec was achieved in the channel. A channel doping of 6 x $10^{16}cm^{-3}$ with the above launcher doping of 3 x $10^{17}cm^{-3}$ represents a launcher/channel doping ratio of five, one-half to one-third that of those studied in this work. Furthermore, an increased channel doping is consistent with the need to reduce the parasitic channel series resistance, to reduce the electric field in the channel, and to improve the device output characteristics. Additional quantitative analysis of the type done by Al-Omar et al. [8] should be used to optimize launcher channel designs for future experimental investigation.

Because it ameliorates many of the problems inherent in the device structure of this work, and as a vertical device amenable to the incorporation of hot-electron injection structures in the source (emitter), the Permeable Base Transistor may be an appropriate vehicle to further develop the device concepts which were the basis of this work. Before an experimental effort is undertaken towards this end, however, experiment on the source-down structure should be carried out and more one-dimensional, two-terminal and two-dimensional, three-terminal simulations are necessary to verify, in particular, that an appropriate forward bias conduction band profile may be achieved in the PBT structure.

Experimental evidence of electron velocity enhancement by hot-electron injection into the channel of a GaAs vertical FET has been successfully obtained for the first time with source down. Electrons are rapidly accelerated by an n^+-i-p^+-i-n^+ planar-doped-barrier launcher and transport nonequilibriumly through a thin

channel at a very high speed. The doping density and thickness of the planar-doped barrier have been designed by use of a one-dimensional computer simulator. The channel thickness has been reduced to 0.13 μm in order to decrease the energy loss of electrons in the channel due to scattering with optical phonons. The source parasitic resistance has been minimized by the overlapped gate-on-launcher structure and the drain-up structure. The maximum transconductance observed and the average electron velocity evaluated are 234 mS/mm and 6.4 x 10^7cm/s, which are 1.4 and 1.9 times as large as those of a conventional vertical FET with the same doping and dimensions, respectively.

Electron energy distribution on the drain edge of a channel in a non-gated vertical FET with hot-electron injection has been determined by using planar-doped-barrier as an electron energy analyzer. Although there is no evidence of ballistic transport, the electron temperature is dramatically increased, up to 1000°K, with increasing drain current. The high electron temperature is mainly due to the hot-electron injection, and it results in increasing the average electron velocity and transconductance.

Motivated by the lack of encouraging transistor performance in the heterojunction (AlGaAs/GaAs) launcher containing vertical FET's previously studied, research during the final phase of this project was directed towards an investigation of the homojunction planar-doped barrier (PDB) and its performance in the vertical FET structures of this work. The fabrication technology for the PDB-containing devices is the same as that for the heterojunction-

containing devices and has been previously described. Additionally, the effect of gate placement relative to the launcher was investigated in the PDB-containing devices.

I.D. DETAILED RESULTS FOR PART 1

1. Device Processing (Source Up)

1.1 The Planar-Doped Barrier Launcher

A thin sheet of charge formed by a depleted donor or acceptor layer in a bulk semiconductor induces band bending in the structure contributing to the formation of a barrier. The first report of this concept was by Shannon [1] in his invention of the camel diode formed by the implantation of a thin p^+-layer into a bulk n-type Si substrate. Because the p^+-layer is fully depleted of holes, the camel diode is a majority carrier device whose frequency of operation is not limited by charge storage effects and whose current transport is not limited by minority carrier diffusion.

Shortly after the report of Shannon's camel diode, Malik et al. [2] introduced another majority carrier diode termed the planar-doped barrier (PDB). A variation on the camel diode, the planar-doped barrier was implemented in GaAs and was designed to exploit the doping and thickness control possible using MBE. The PDB diode consists of a fully depleted p^+-plane of acceptors located within an intrinsic region sandwiched by n^+-regions. The representative doping profile, charge distribution, electric field distribution, and potential profile for a PDB diode are shown in Figure1. The barrier height resulting from this structure can be continuously varied from zero to nearly the band gap of the material by adjusting the sheet

charge of the p^+-layer. Furthermore, the barrier shape may be significantly tailored by the choice of the lengths L_1 and L_2 in Figure 1.

The PDB structure studied in this work is modified for high current density operation by minimizing the lengths of the intrinsically doped regions. The resulting design approaches that of Shannon's camel diode in that the camel diode can be considered a PDB in the limit that the intrinsically doped regions have been reduced to zero. One of the PDB epilayer structures, typical of the several attempts made near the conclusion of this work, grown by MBE (run #2685) is diagrammed in Figure 2. The PDB launcher consists of five layers of GaAs, 250 Å doped at $2 \times 10^{17} cm^{-3}$, n-type, 35 Å, intrinsically doped, 50 Å doped at $5 \times 10^{18} cm^{-3}$, p-type, 85 Å, intrinsically doped, and 150 Å doped at $2 \times 10^{18} cm^{-3}$, n-type. The thin intrinsically doped regions serve primarily as diffusion barriers/spacers between the heavily doped regions. The latter n^+-layer is kept as thin as possible to minimize impurity scattering immediately downstream of the launch plane.

The zero bias conduction band diagram calculated for this structure is shown in Figure 3. The calculated zero bias barrier height is seen to be 0.28 V. At first, this barrier height would seem to be just as desired. Unfortunately, however, the effective injection energy of a PDB launcher increases by a fraction of the applied forward bias due to a leverage effect in the structure. In this case, the effective injection energy would be on the order of 0.40 eV at near flat band bias. Alternately, one would have liked to

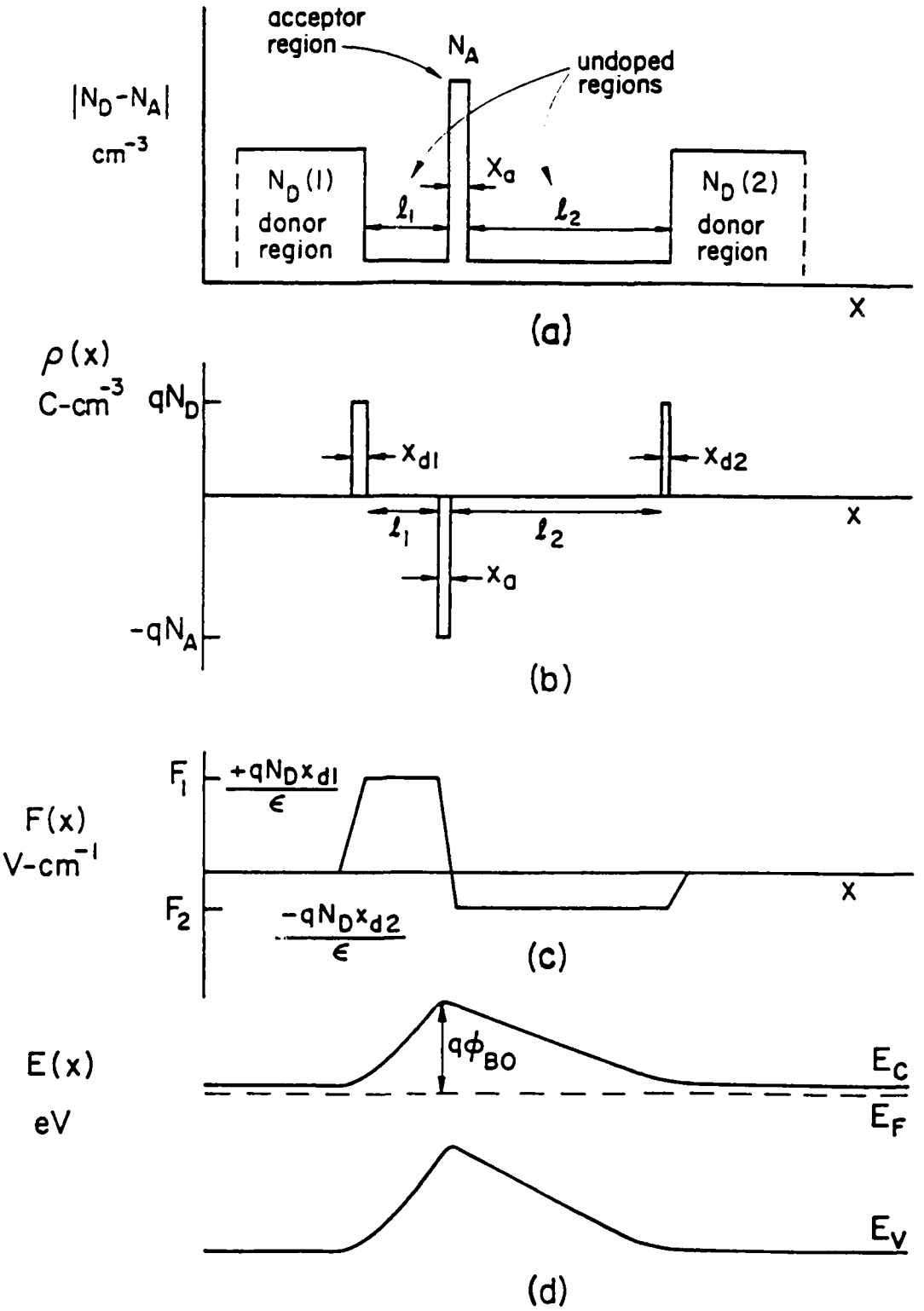

Figure 1. (a) Doping profile, (b) charge distribution, (c) electric field distribution, and (d) band diagram of a planar-doped barrier structure at zero bias.

2500 Å n^+ GaAs	$2X10^{18}$ cm^{-3}	SOURCE
2500 Å n GaAs	$2X10^{17}$ cm^{-3}	PLANAR
35 Å i GaAs	UNDOPED	DOPED
50 Å p^+ GaAs	$5X10^{18}$ cm^{-3}	
85 Å i GaAs	UNDOPED	BARRIER
150 Å n^+ GaAs	$2X10^{18}$ cm^{-3}	
0.5 μm n^- GaAs	$2X10^{16}$ cm^{-3}	CHANNEL
2.0 μm n^+ GaAs	$2X10^{18}$ cm^{-3}	DRAIN
SI GaAs SUBSTRATE		

Figure 2. Epilayer structure for the planar-doped barrier launcher device, layer #2685.

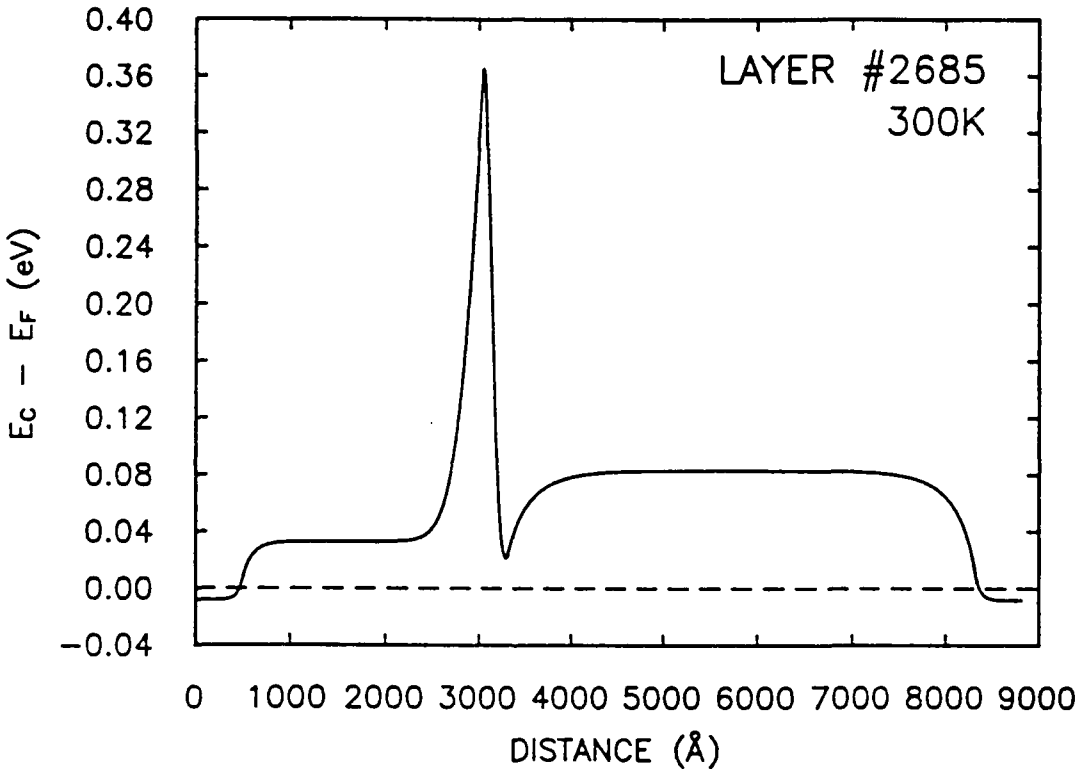

Figure 3. Zero bias, 300°K conduction band diagram for the planar-doped barrier launcher device, layer#2685.

design for a zero bias barrier height of no more than about 0.20 V.

The typical room temperature source-drain I-V characteristic for this structure is shown on a linear scale in Figure 4 and on a semilog scale in Figure 5. The linear I-V of Figure 4 shows significant rectification with a turn-on voltage of ~0.25 V. From the linear region of Figure 5, f_{BO} is determined to be 0.27 V in excellent agreement with the theoretical value of 0.28 V. The agreement between the measured and theoretical values for f_{BO} indicate that the MBE growth was well-calibrated. The ideality factor for this structure is 1.84. The measured room temperature saturation current density is in the range of 7.6 kA/cm^2 to 29.0 kA/cm^2, depending on the placement of the gate relative to the PDB launcher. The value of 29.0 kA/cm^2 is for the gate well-astride the PDB launcher and is the highest value for any of the launchers studied, approaching the desired value of 100 kA/cm^2. The increase in J_{sat} with increasing gate-launcher overlap is attributed to the reduction of channel-narrowing surface depletion effects. With the gate overlapping the launcher, there is no exposed surface on the lightly-doped channel and the full open-channel current density may be achieved. The effect of gate placement relative to the PDB launcher on transistor performance will be covered in section I.E.

The slight over design of the PDB launchers studied in this work can be partly understood by looking at the dependence of the zero bias barrier height on the sheet charge density of the p^+-layer and of the n^+-layer.

The variation of f_{BO} with the sheet charge density, s_p, of the

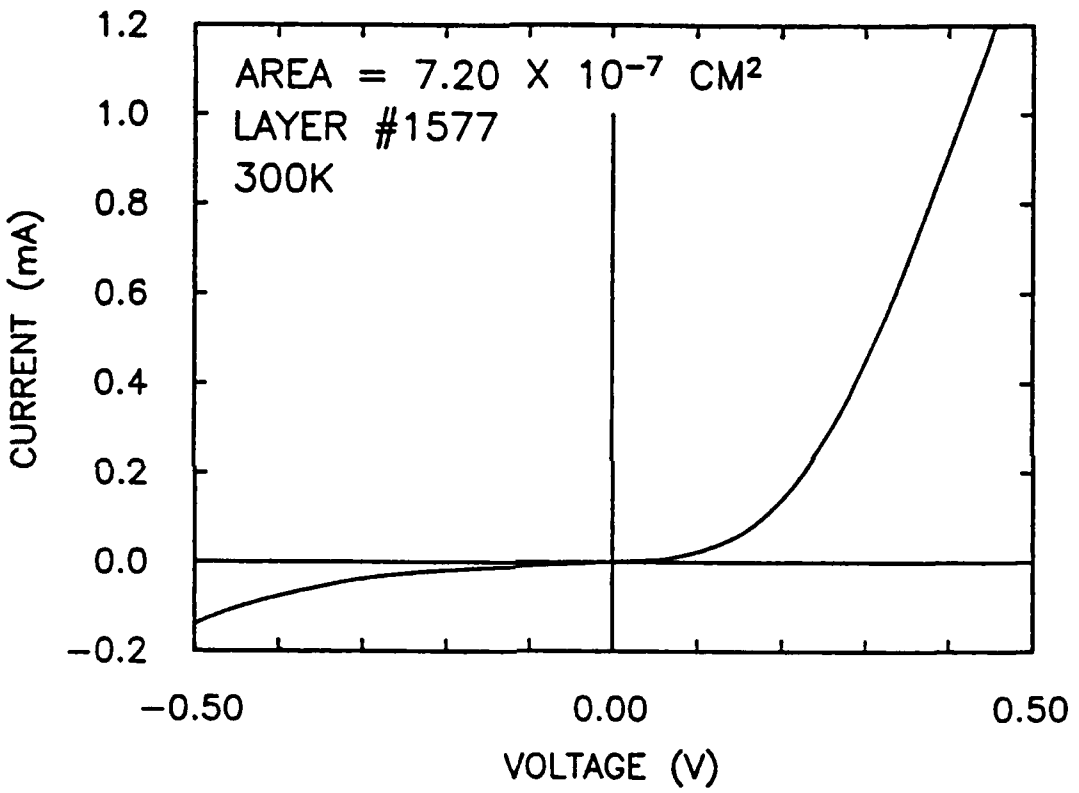

Figure 4. Source-drain I-V characteristic at 300°K for the planar-doped barrier launcher device on a linear scale.

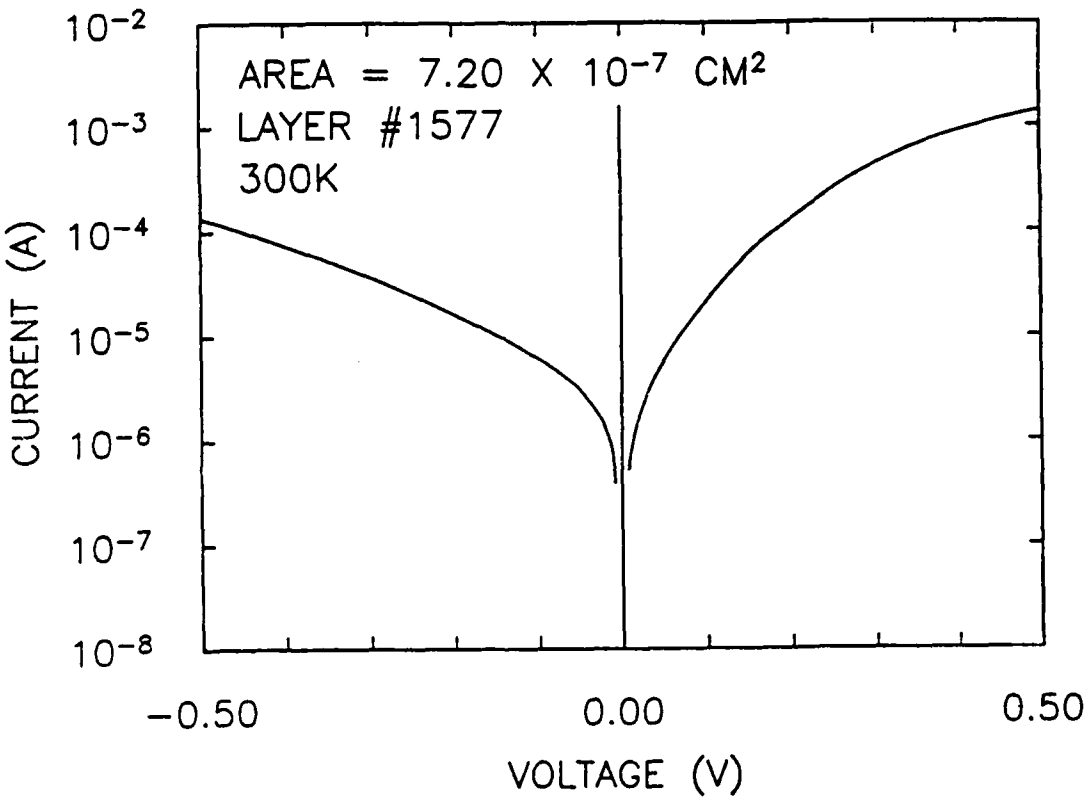

Figure 5. Source-drain I-V characteristic at 300°K for the planar-doped barrier launcher device on a semilog scale.

p^+-layer in the structure of Figure 2 is shown in Figure 6. This curve was generated by calculating the conduction band diagram for the structure of Figure 2 for eight different p^+-layer sheet charge densities in the range 5 to 50 x $10^{11}cm^{-2}$ and joining the resulting discrete f_{BO} data points with a smooth line. The zero bias barrier height is seen to vary quite rapidly across the range of sheet charge density. A variation of 20% in the sheet charge density in the region where f_{BO} = 0.20 V results in a 33% change in f_{BO}.

In the conventional PDB, the n^+-layers which sandwich the PDB structure are much thicker than the width of the depletion regions at the edges of the n^+-layers. As a result, the n^+-layers only affect the barrier height to the extent that they fix the position of the conduction band relative to the Fermi level in the regions adjacent to the depletion regions. For most levels of n^+ doping, the conduction band will be within tens of meV of the Fermi level. In the modified PDB, however, the downstream n^+-layer is sufficiently thin to be largely depleted for the range of doping-thickness products considered and the conduction band does not achieve the equilibrium position it would in an equivalent bulk n^+-layer. Instead, a potential well is formed between the barrier peak and the n^--drift region, the depth of which varies with the doping-thickness product of the n^+-layer. The depth of the well, in turn, affects the height of the barrier both at zero bias and under forward bias since a barrier not pinned to the Fermi level will exhibit a greater leverage effect. The variation of f_{BO} with the doping-thickness product, N_t, of the downstream n^+-layer in the structure of Figure 2 is shown in Figure 7. As above, this curve was generated by calculating the

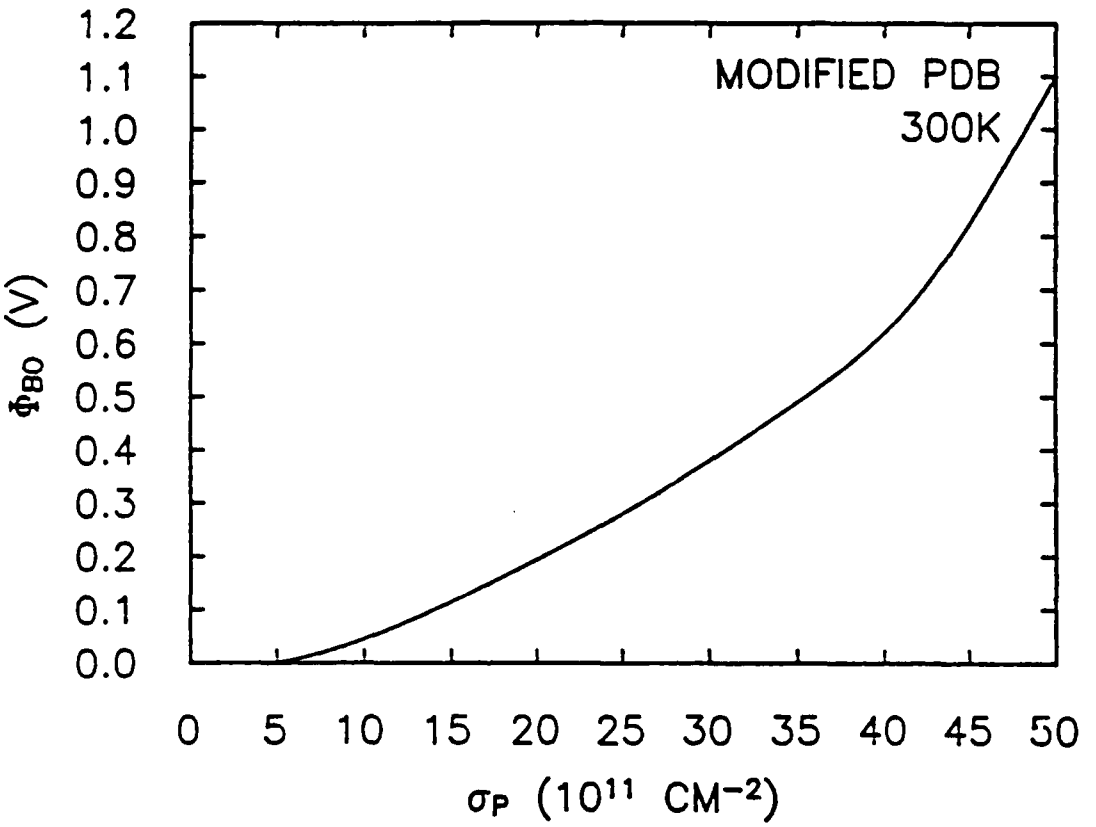

Figure 6. Zero bias barrier height versus sheet charge density of the p^+-layer for the PDB structure of Figure 2 at 300°K.

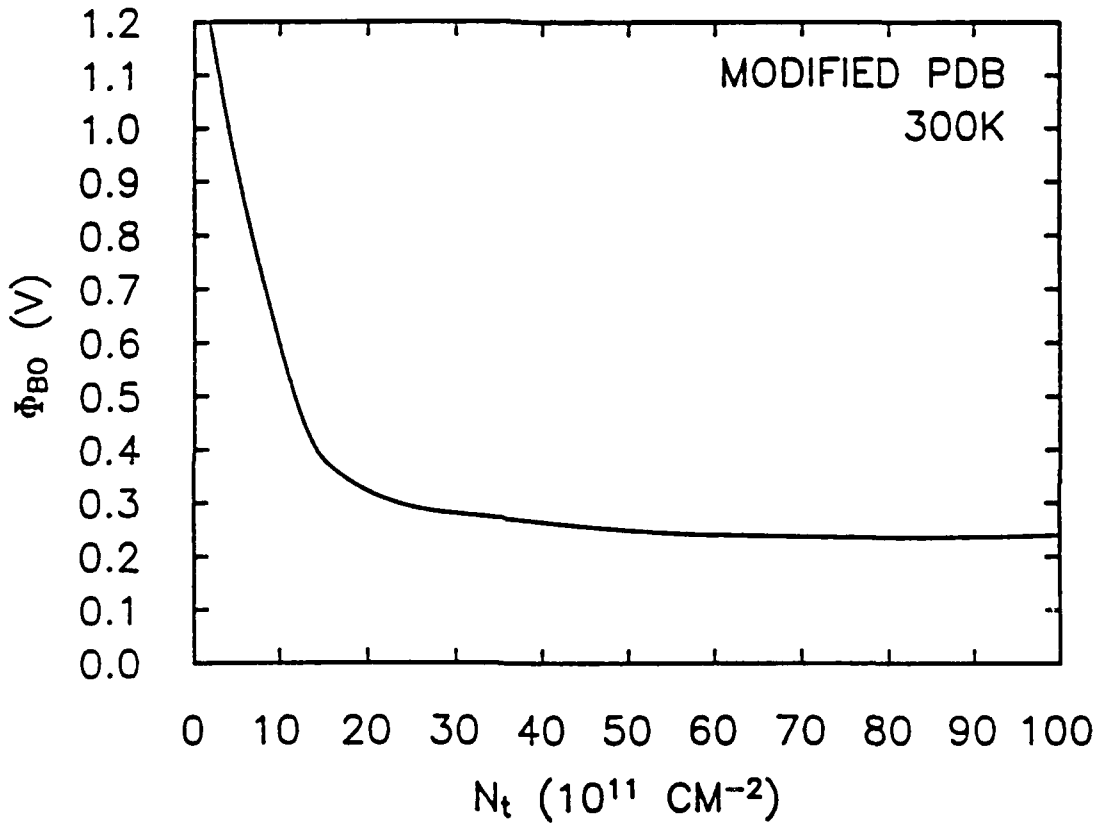

Figure 7. Zero bias barrier height versus doping-thickness product of the downstream n^+-layer for the PDB structure of Figure 2 at 300°K.

conduction band diagram for several discrete doping-thickness products of the downstream n^+-layer in the structure of Figure 2. The zero bias barrier height is seen to be constant for values of N_t greater than 50 x $10^{11}cm^{-2}$ as the well rises up, away from the Fermi level. Part of the reason, then, for the larger than desired barrier heights of the PDB launchers grown in this work can be attributed to the use of too small a doping-thickness product in the downstream n^+-layer (30 x $10^{11}cm^{-2}$). The use of a slightly higher value of N_t would be expected to have reduced fLBO by 0.04 V or ~15%.

1.2 Vertical FET's with Planar-Doped Barrier Launchers

The epilayer structure and zero bias conduction band profile for the planar-doped barrier launcher devices (layer #2685) have been previously shown in Figures 2 and 3, respectively. The zero bias barrier height of the launcher was measured to be 0.27 V. All of the PDB launcher devices fabricated were of the conventional cross section structure but the gate placement with respect to the launcher was quantitatively varied across the wafers.

Wafers intended for the study of gate placement relative to the launcher underwent a surface profile modification [3]. These wafers were grown with an extra thick n-region in the source to allow for the removal of 500 to 1000 Å of material from selected macroscopic regions of the wafer resulting in the formation of a

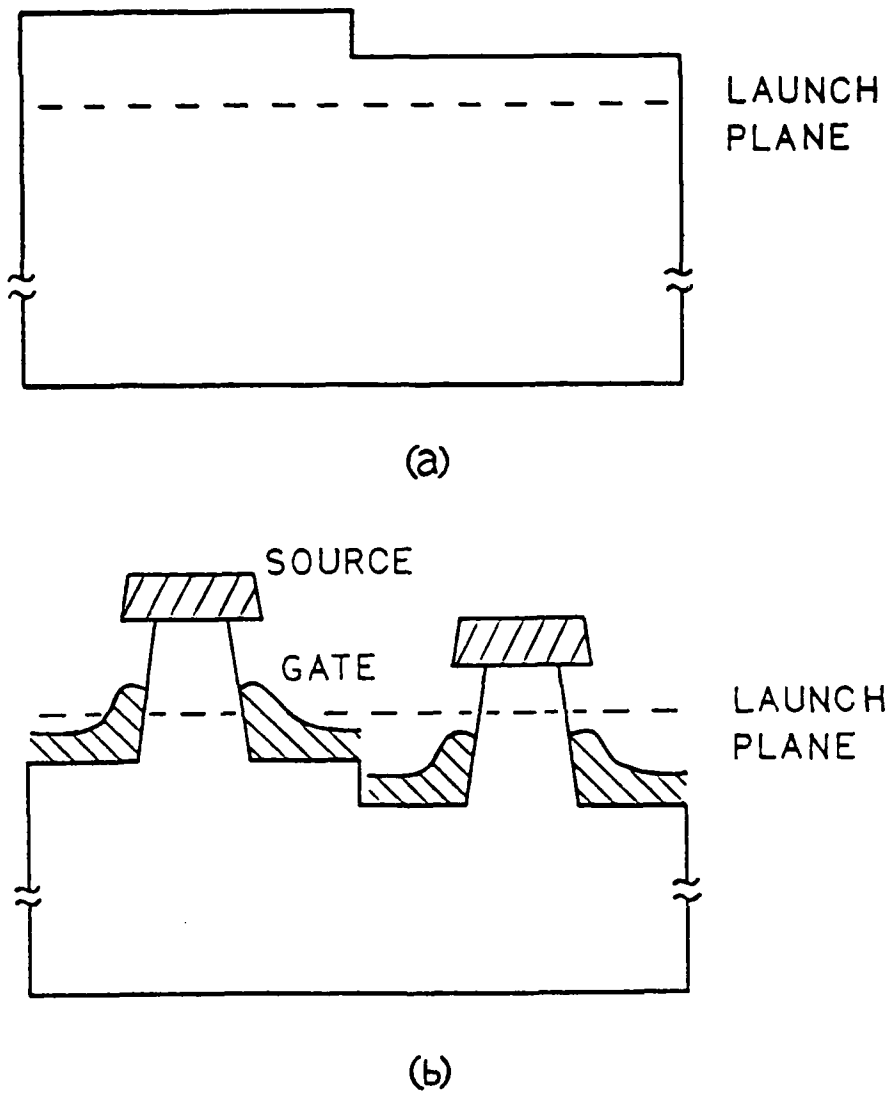

Figure 8. Wafer surface profile modification to vary gate placement with respect to the launcher. (a) Surface profile after level L(-1). (b) Wafer cross section after gate deposition.

stepped surface profile as indicated schematically in Figure 8a. The stepped profile is simply achieved by masking a given region with photoresist and using the slow, well-behaved (1:2:1):200::(NH_4OH:H_2O_2:H_2O):H_2O etch to remove material from the unmasked area. Afterwards, the step height is measured using a Tencor Alpha-Step 100 profilometer. The effect of this stepped profile is to place the launcher at different depths from the surface and when after subsequent processing the gate is deposited, the gate position relative to the launcher varies from region to region exactly by the amount of the step between the regions as shown schematically in Figure 8b.

1.2.1 Effects of Gate Placement Relative to the PDB Launcher

Motivated by the mediocre performance of devices with nominal 1000 Å gate-source spacings and by growing concern towards the appropriateness of attempting to modulate injected energetic electrons by a downstream depletion region, it was proposed to deposit the gate partly overlapping on the launcher in hopes of more directly modulating the flow of injected electrons. In practice, a range of gate placements relative to the launcher was investigated corresponding to values of both positive and "negative" overlap where the quantitative overlap is defined relative to the launch plane as indicated in the schematic representations of Figure 9. "Negative" overlap is seen to correspond to a positive gate-source spacing. Additionally, the qualifying terms "below", "at", and "on"

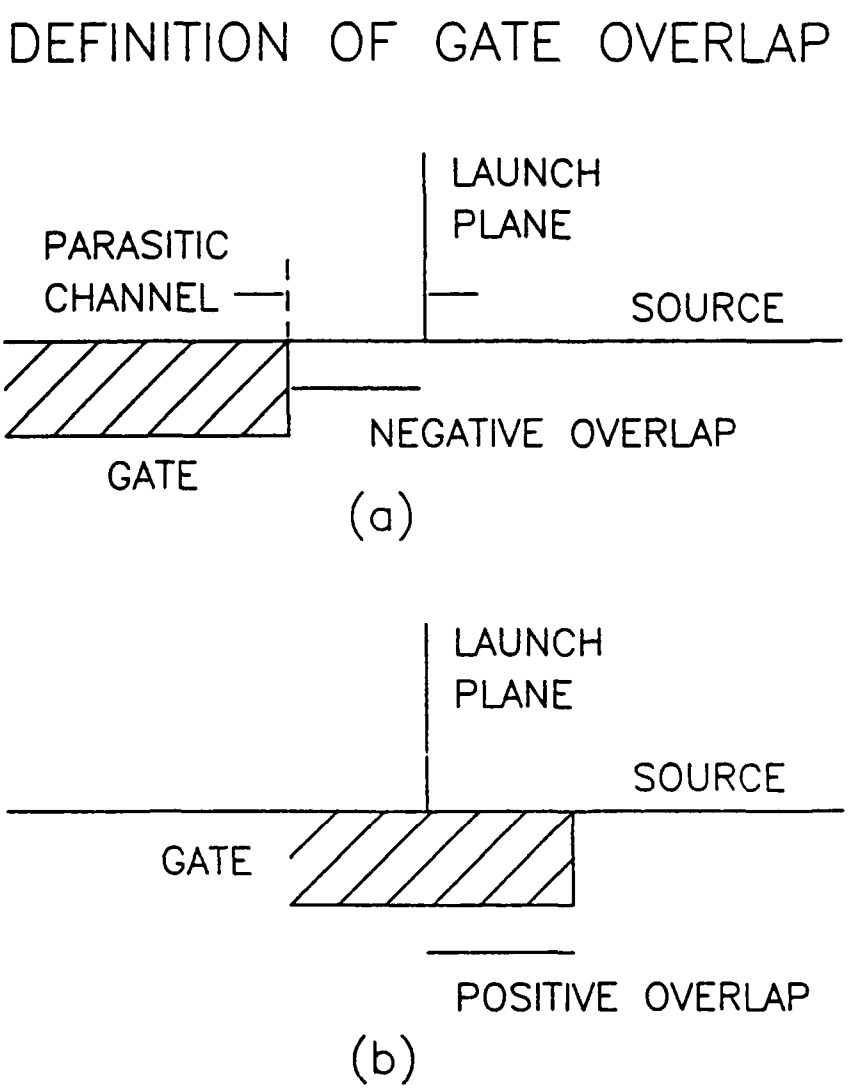

Figure 9. Schematic representations defining the quantities (a) negative overlap and (b) positive overlap.

[the launcher] will be used during subsequent discussion and are largely self-explanatory with the exception of "at" [the launcher] which refers to the 700 Å region from 200 Å below the launch plane to 500 Å above the launch plane, or put differently, the 200 Å on each side of the PDB launcher plus the 300 Å of the PDB launcher, itself. The regions associated with these qualifying terms are indicated in Figures 14, 15, 16 and 17.

Representative room temperature transistor I-V characteristics for vertical FET's of 144 μm gate width with planar-doped barrier launchers and gate-launcher overlaps of - 800 Å (below), 500 Å (at), 1000 Å (on) are shown in Figures 10, 11, 12 and 13, respectively. The data came from two device runs from the same wafer (#2685(2) and #2685(3)) where the number in parentheses distinguishes the device run. A turn-on voltage of 0.25 V is evident, consistent with the measured launcher barrier height.

There are many interesting trends evident in this series of characteristics. For example, one trend which is both evident and expected is an increase in the gate-drain breakdown voltage with increasing gate overlap consistent with the fact that the gate-drain spacing is also increasing. The approximate values of the gate-drain breakdown for Figures 10, 11, 12 and 13 are 1.75 V, > 3.5 V, 6.25 V, and > 7.5 V, respectively. No problems with gate-source breakdown were observed even for gates which fully overlapped the launcher. This is due in large part to the inclusion of the 2500 Å layer of n-type GaAs doped at $2 \times 10^{17} cm^{-3}$ between the launcher and n^+-source contact layer which provides room for the gate to overlap the

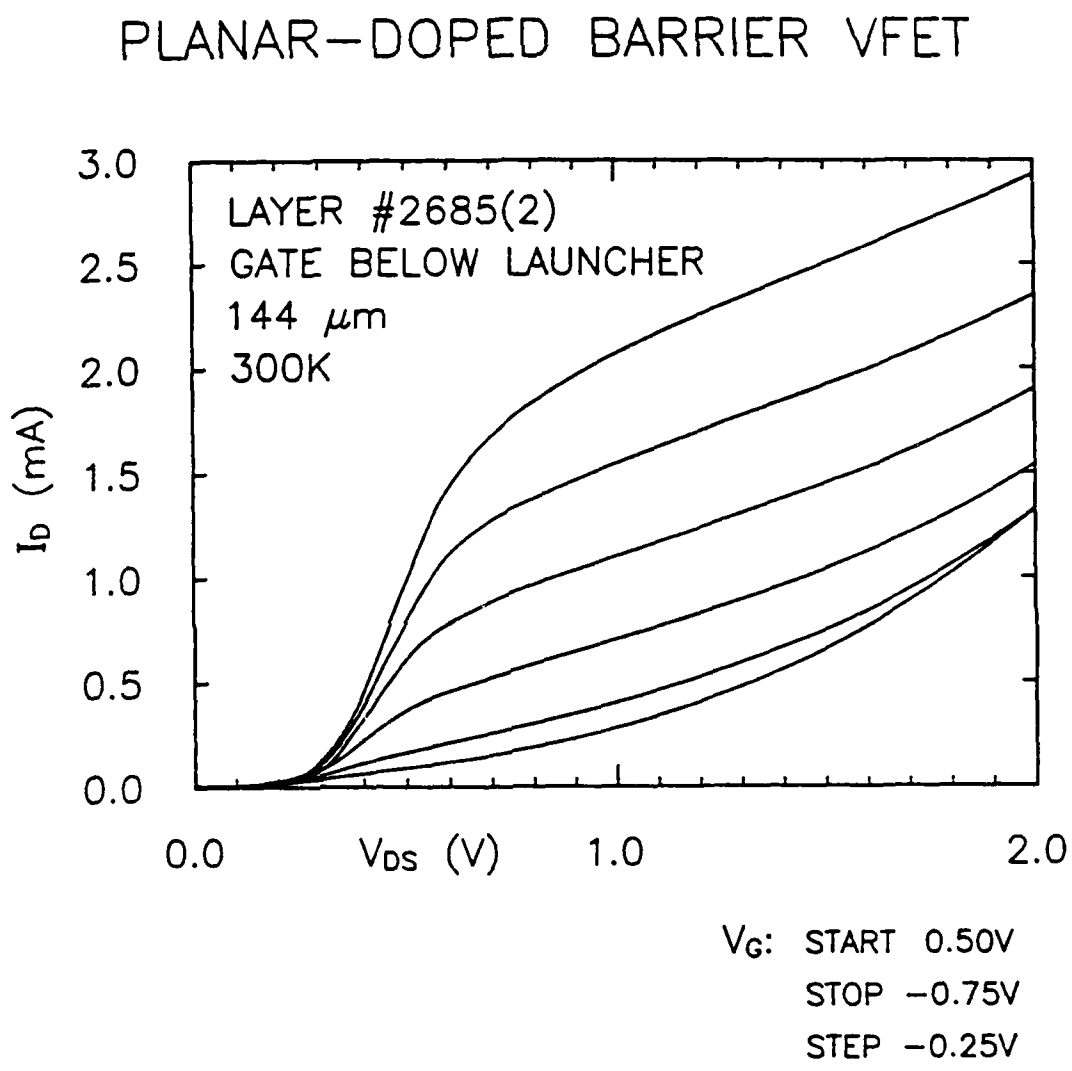

Figure 10. Transistor I-V characteristic at 300°K for a vertical FET with planar-doped barrier launcher and -800 Å gate overlap.

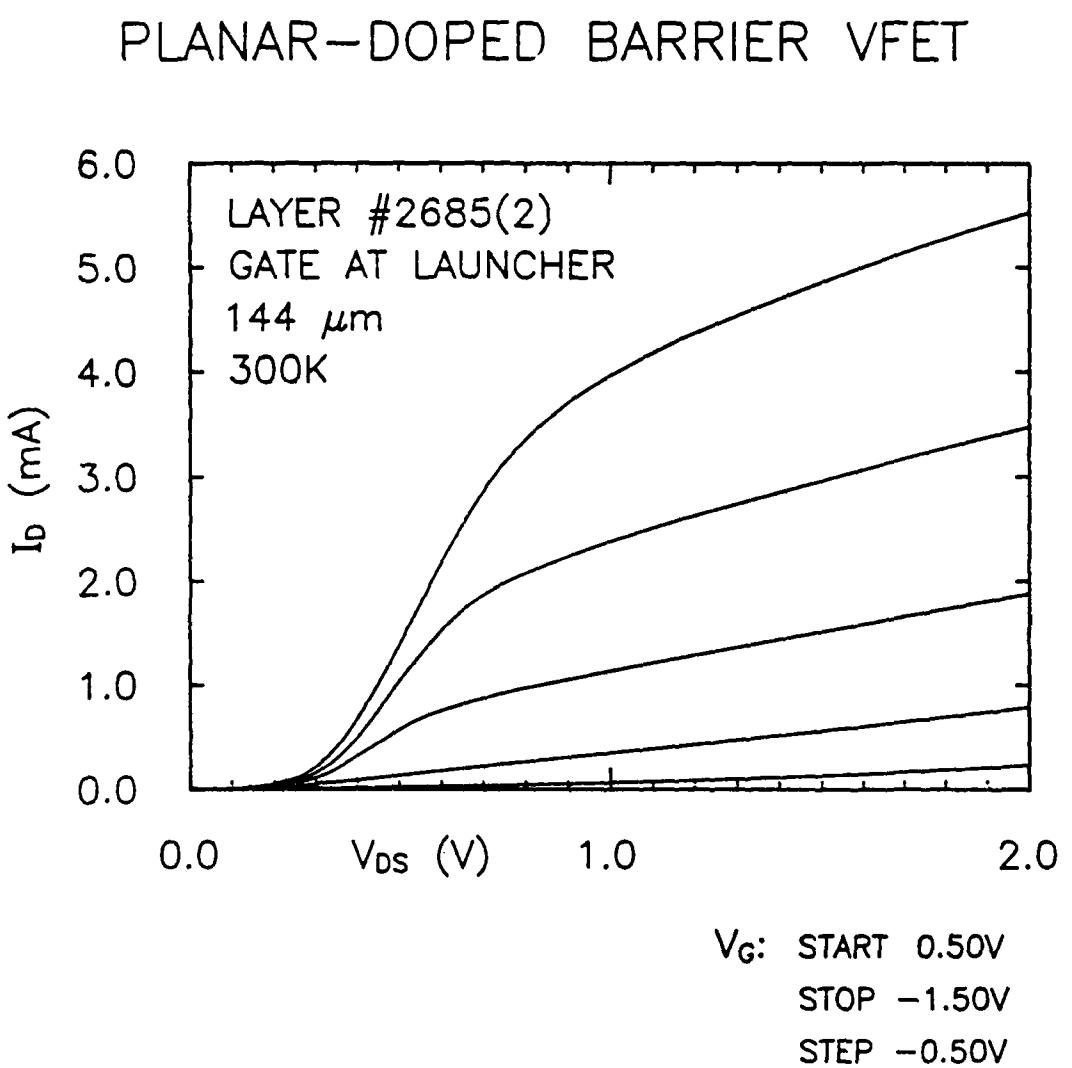

Figure 11. Transistor I-V characteristic at 300°K for a vertical FET with planar-doped barrier launcher and 500 Å gate overlap.

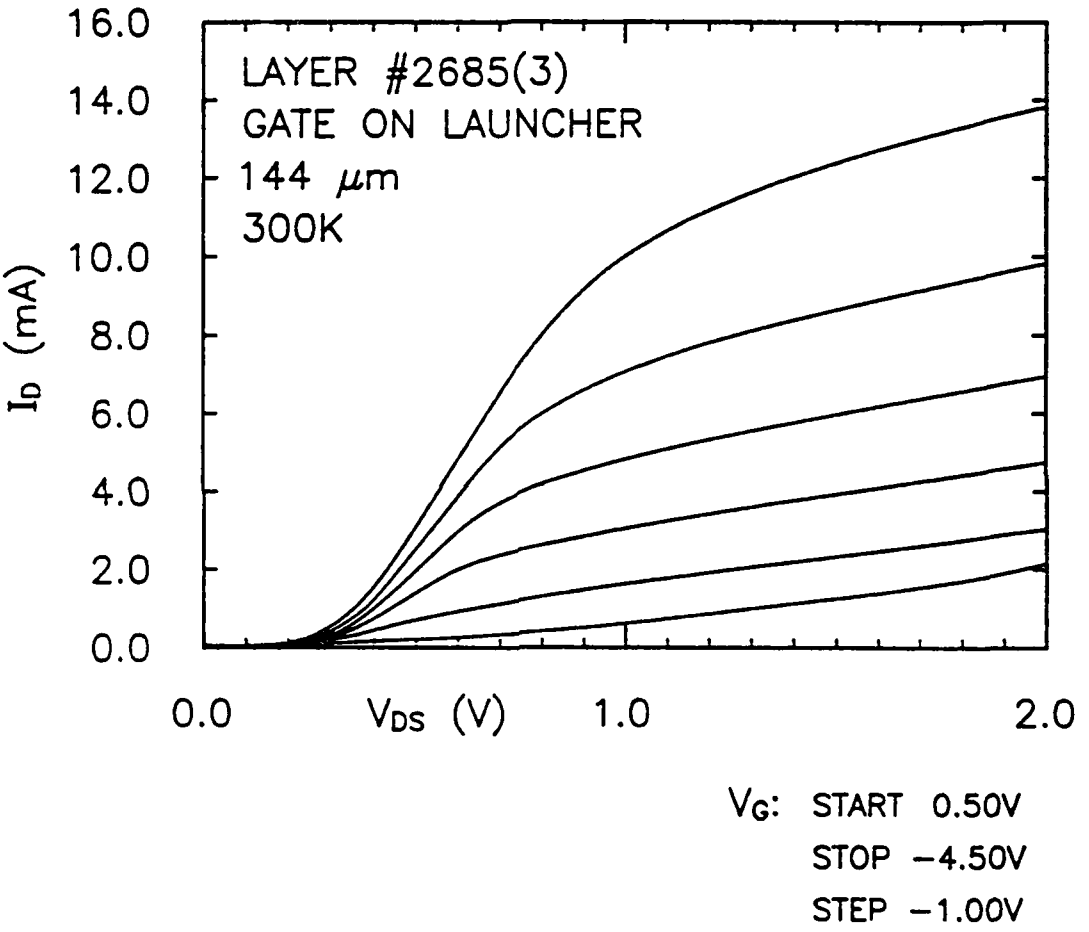

Figure 12. Transistor I-V characteristic at 300°K for a vertical FET with planar-doped barrier launcher and 1000 Å gate overlap.

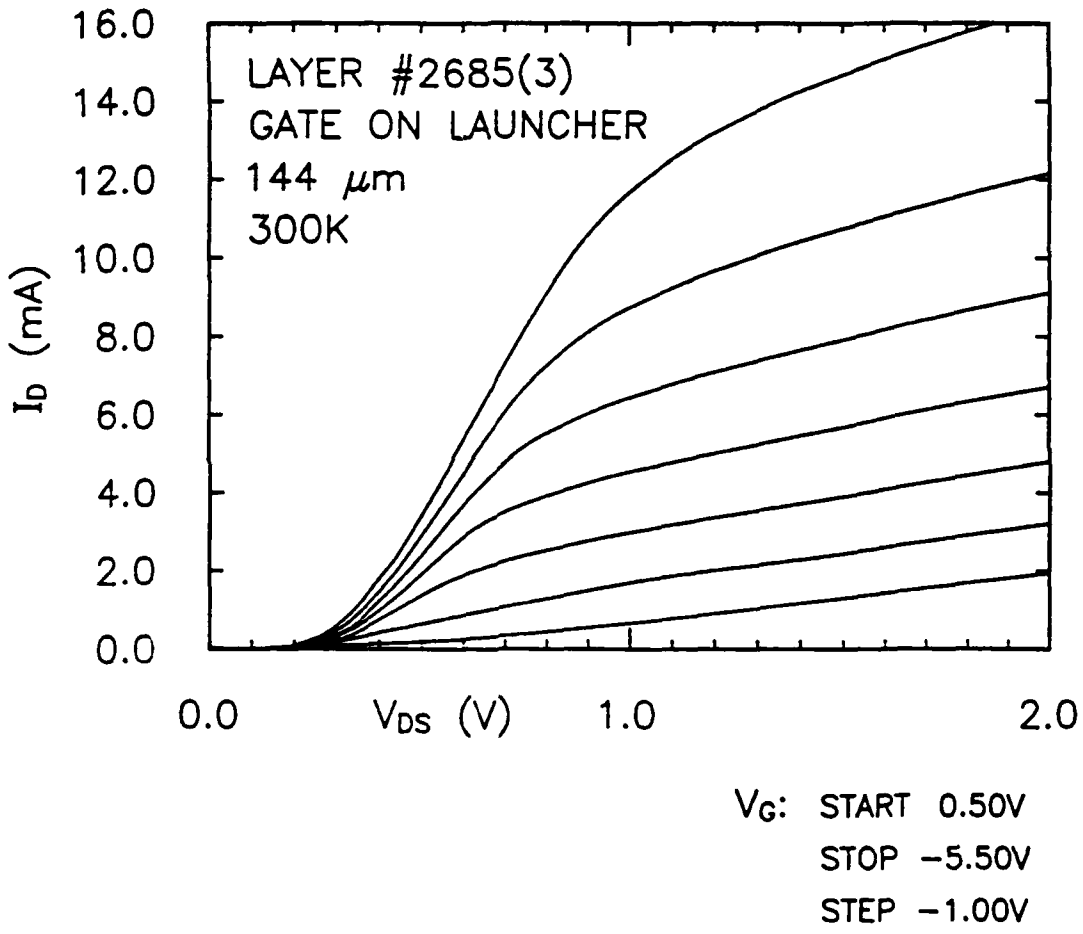

Figure 13. Transistor I-V characteristic at 300°K for a vertical FET with planar-doped barrier launcher and 1670 Å gate overlap.

source without contacting the heavily doped n^+-source contact layer.

More evident, perhaps, is the increase in open-channel saturation current and in device threshold voltage with increasing overlap. It must be noted that the marked jump in I_{DS} and V_T between the characteristics of Figures 11 and 12 is due to the difference in channel width between runs #2685(2) and #2685(3), 0.31 μm versus 0.62 μm, respectively. This channel width difference may be accounted for by calculating the open-channel saturation current densities, J_{sat}, for each of the characteristics and which are shown plotted as a function of gate overlap in Figure 14. Here, J_{sat} is seen to increase uniformly with increasing gate overlap consistent with a decreasing effective source resistance expected as the size of the parasitic channel is first reduced and then eliminated once positive gate overlap has been achieved.

The specific source and drain resistances are plotted as a function of gate overlap in Figure 15. Again, to account for the channel width difference between the two device runs, the measured source and drain resistances were converted to specific source and drain resistances by multiplying the values by the respective device active areas. The behavior of the specific source resistance is again consistent with the initial decrease in the size of the parasitic channel as the gate approaches the launcher followed by its elimination once the gate actually overlaps the launcher. The variation in specific drain resistance with gate overlap is much less dramatic, as expected, since the drain resistance increases only as the result of the slight increase in gate-drain spacing as the gate is moved up the channel.

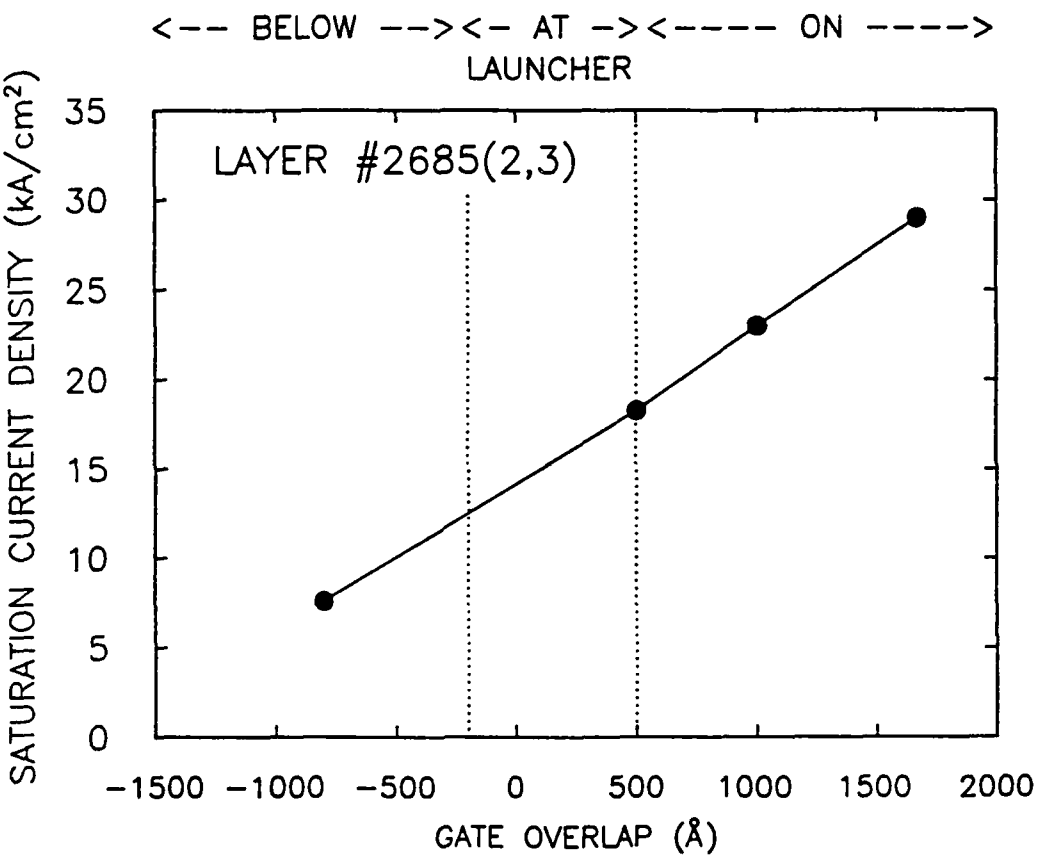

Figure 14. Plot of saturation current density versus gate overlap for PDB layers #2685(2,3).

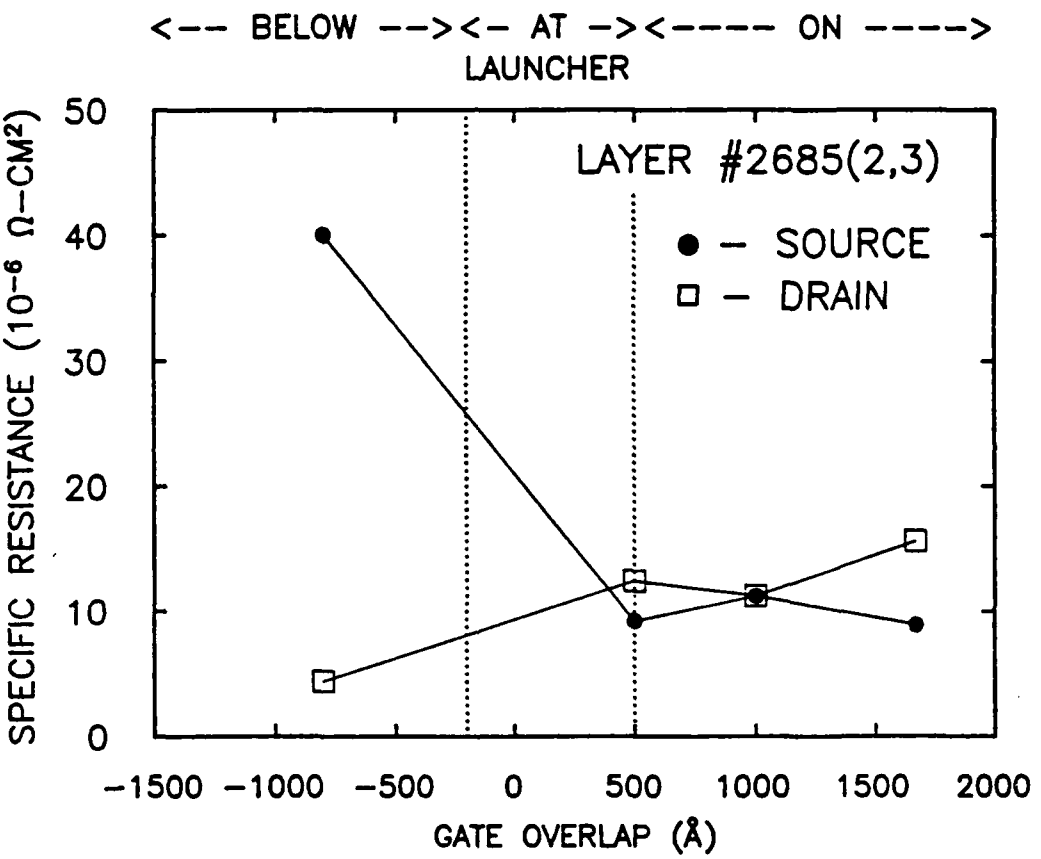

Figure 15. Plot of specific source and drain resistances versus gate overlap for PDB layers #2685(2,3).

The extrinsic and intrinsic transconductances, g_m and g_{mo}, respectively, normalized to gate width, are plotted as a function of gate overlap in Figure 16. The behavior of the extrinsic transconductance would at first seem to indicate a marked improvement in the current modulation capability of the gate with increasing gate overlap. When this curve is corrected for differences in source resistance to generate the curve of intrinsic transconductance, however, the degree of improvement with increasing gate overlap is greatly diminished. Only this remaining, relatively meager improvement in intrinsic gm may be attributed to any improvement in gate modulation and even then the improvement can also be easily explained simply by the increase in free charge underneath the gate as it moves higher up the channel and begins to overlap the more highly-doped source region.

Furthermore, not only does the problem of significant output conductance persist throughout the characteristics of Figures 10, 11, 12 and 13, indicating the continued presence of space-charge limited current flow beyond geometrical pinch-off, but the output conductance actually increases with increasing gate overlap. This behavior is revealed in the plot of drain conductance, g_D, versus gate overlap in Figure 17 and can be understood by considering that as the gate moves up the channel and out of the region between the source and drain, what shielding the gate provided when astride the channel is necessarily diminished when the gate is barely even between the source and drain. It must gain be noted that the marked jump in g_D between the values of gate overlap of 500 Å and 1000 Å is

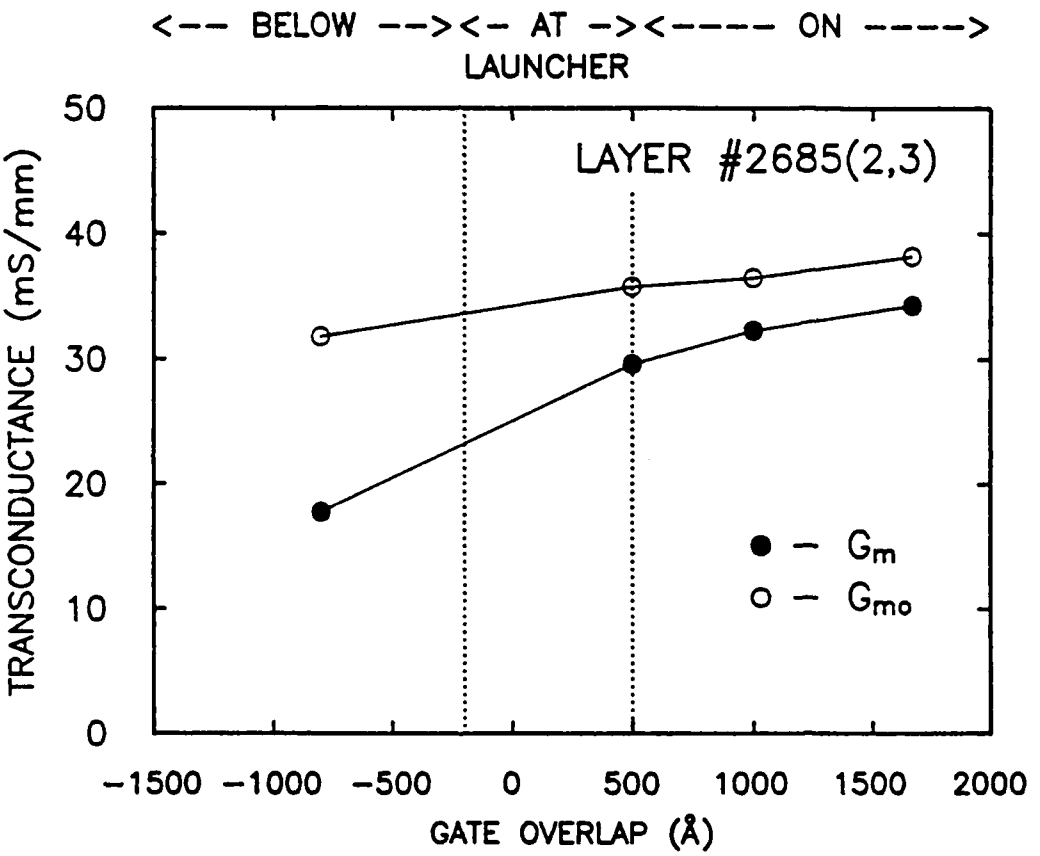

Figure 16. Plot of extrinsic and intrinsic transconductances versus gate overlap for PDB layers #2685(2,3).

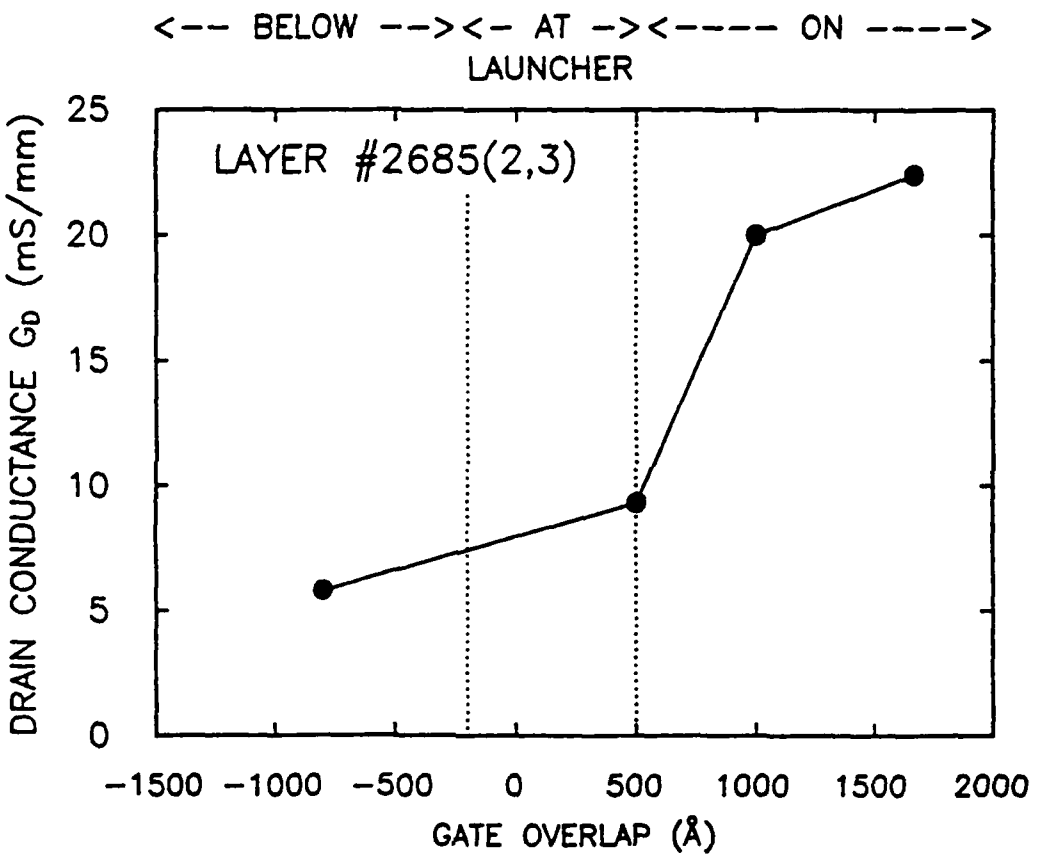

Figure 17. Plot of drain conductance versus gate overlap for PDB layers #2685(2,3).

attributed to the difference in channel width between runs #2685(2) and #2685(3).

The original goal of the gate-on-launcher concept to achieve direct launcher modulation with the promise for improved device performance has not been realized. What has been illustrated is the current-limiting effect of the surface depletion of the parasitic channel and, therefore, the importance of minimizing the size of the parasitic channel region in devices with lightly-doped channels.

2. Device Processing (Source Down)

2.1 Introduction

Hot electron injection into a FET channel is a very attractive concept for very high speed electron devices, because it can increase the average electron transit velocity, transconductance and cut-off frequency. However, previous experimental results did not demonstrate any apparent velocity enhancement. The possible reasons for these disappointing results are considered to be as follows:

1. The channel thickness (about 0.5 μm) was too large for electrons to be transported ballistically, because a mean free path for hot electrons, determined by recent theoretical calculations and direct experiments of hot electron spectroscopy is 30-40 nm in 1 x $10^{18}cm^{-3}$ n^+ doped layer and about 70 nm in 1 x $10^{17}cm^{-3}$ n doped layer.
2. The material quality of MBE layers with AlGaAs/GaAs heterojunction launchers was not good enough.

3. Source parasitic resistance was large because of the surface depletion of the channel between the source and the gate.

Therefore, the channel thickness was reduced to 0.13 μm and an n^+-i-p^+-i-n^+ planar doped barrier (PDB) was chosen for launcher instead of the heterojunction. In order to minimize the source resistance, the gate metal was overlapped on the launcher and the drain up structure was chosen instead of the source up structure in the previous reports. The dc electrical characteristics of vertical FETs (VFETs) with launcher were compared with those of conventional VFETs without the launcher. The average electron velocity was estimated from the dc characteristics.

Hot electron spectrometers composed of a non-gated VFET with a PDB launcher and a PDB analyzer were also fabricated by using the similar technology as that of VFETs. The electron energy distribution at the drain edge of a channel was determined at 77°K in order to make clear the electron dynamics in the channel.

2.2 VFETs

2.2.1 Epitaxial Layer and Device Structure

The epitaxial layers were grown by MBE on a semi-insulating GaAs substrate in a Varian Gen II machine. A schematic diagram of a cross section of the starting layers is shown in Figure 1a. A thin n^+-i-p^+-i-n^+ PDB was used for the launcher to reduce the series resistance. The doping density and thickness of the channel n layer were $1 \times 10^{17} cm^{-3}$ and 0.13 μm, respectively. The theoretical mean free path of hot electron in this doped channel layer is about 70 nm. Therefore, an injected hot electron is scattered mainly by an optical

n^+	3×10^{18} cm^{-3}	100 nm	
n^+	1×10^{18} cm^{-3}	200 nm	Drain
n	1×10^{17} cm^{-3}	130 nm	Channel
n^+	3×10^{18} cm^{-3}	16 nm	
undoped		3 nm	
p^+	2×10^{18} cm^{-3}	9 nm	Launcher
undoped		5 nm	
n^+	1×10^{18} cm^{-3}	300 nm	
n^+	3×10^{18} cm^{-3}	1000 nm	Source
Semi-insulating Substrate			

Fig. 1a Schematic cross-section of MBE layer structure for fabricating VFETs with launcher.

n^+	3×10^{18} cm^{-3}	100 nm	Drain
n^+	1×10^{18} cm^{-3}	200 nm	
n	1×10^{17} cm^{-3}	130 nm	Channel
n^+	1×10^{18} cm^{-3}	300 nm	Source
n^+	3×10^{18} cm^{-3}	1000 nm	
Semi-insulating Substrate			

Fig. 1b Schematic cross-section of MBE layer structure for fabricating conventional VFETs without launcher.

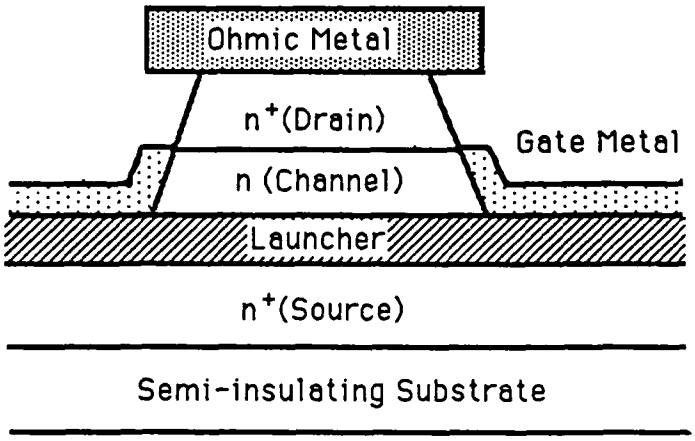

Fig. 1c Schematic cross-section of a single post of a multi-finger VFET with launcher.

(LO) phonon about twice on an average during transport through the 130 nm channel and loses energy of about 0.07 eV.

The conduction band diagram and the injected electron energy were calculated for various applied voltages by using a computer program. This program performs a one dimensional numerical solution to Poisson's equation for an arbitrary layer structure. The calculated results are shown in Figures 2a and 2b. The injected electron energy increases from 0.1 eV to 0.3 eV with increasing drain-source voltage. The length of spill-over of electrons from the n^+ layer into the channel is about 0.03 μm.

For comparison, conventional VFETs without a launcher were also fabricated by using the same layer structure except for the PDB launcher, as shown in Figure 1b.

The device structure is schematically shown in Figure 1c. A drain up structure was chosen instead of source up structure for reduction of source parasitic resistance. The gate metal overlaps, partly, the launcher and the drain n^+ layer. This structure can eliminate the surface depletion effects which increase the source and drain parasitic resistances.

2.2.2 Device Fabrication Procedure

The fabrication steps are very similar to the previously reported ones. All lithography was done on a Karl Suss MJB3 contact aligner using mid-UV radiation. The details are described as follows:

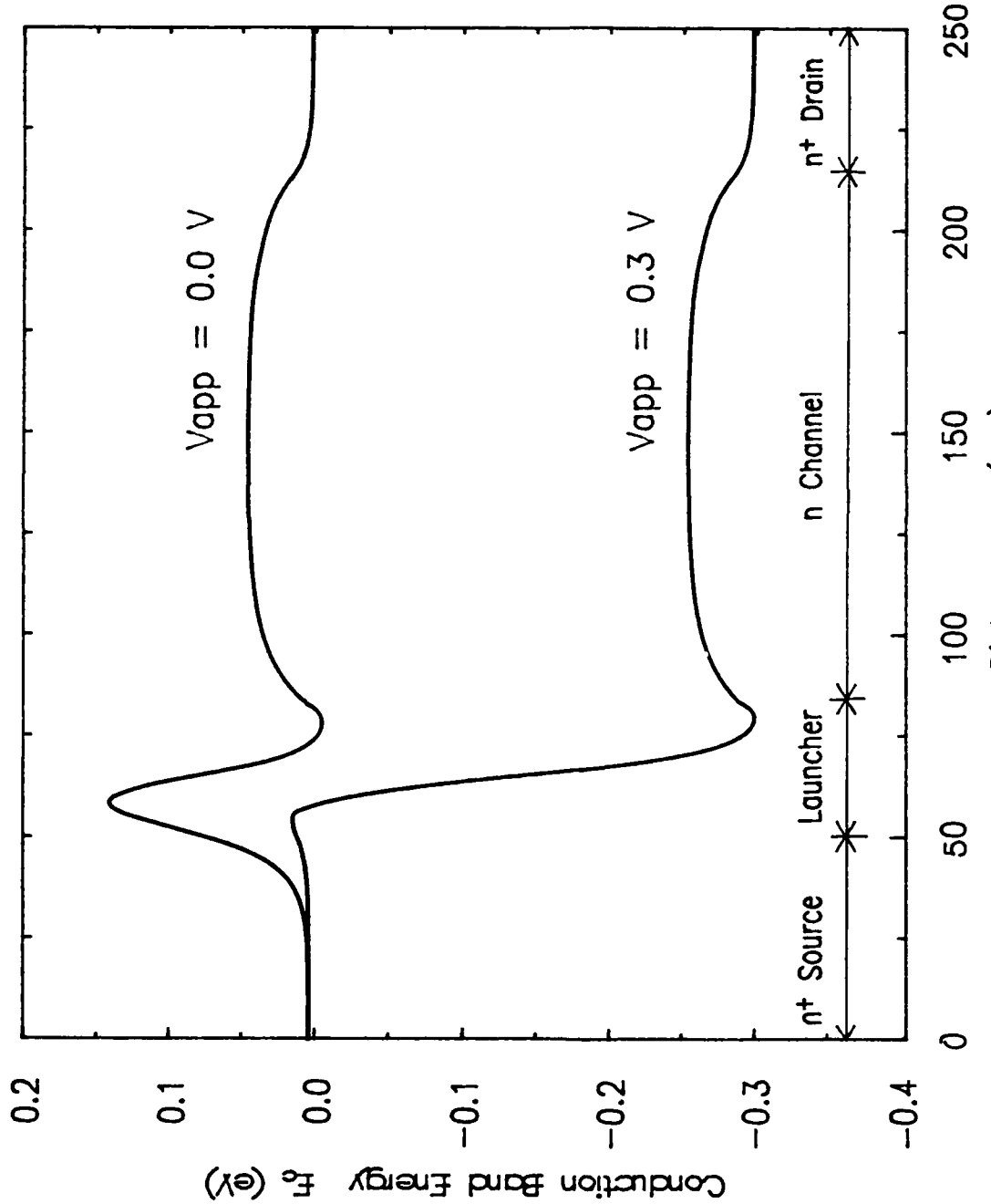

Fig. 2a. Conduction band diagram of VFET with launcher at 0.0 V or 0.3 V of applied voltages.

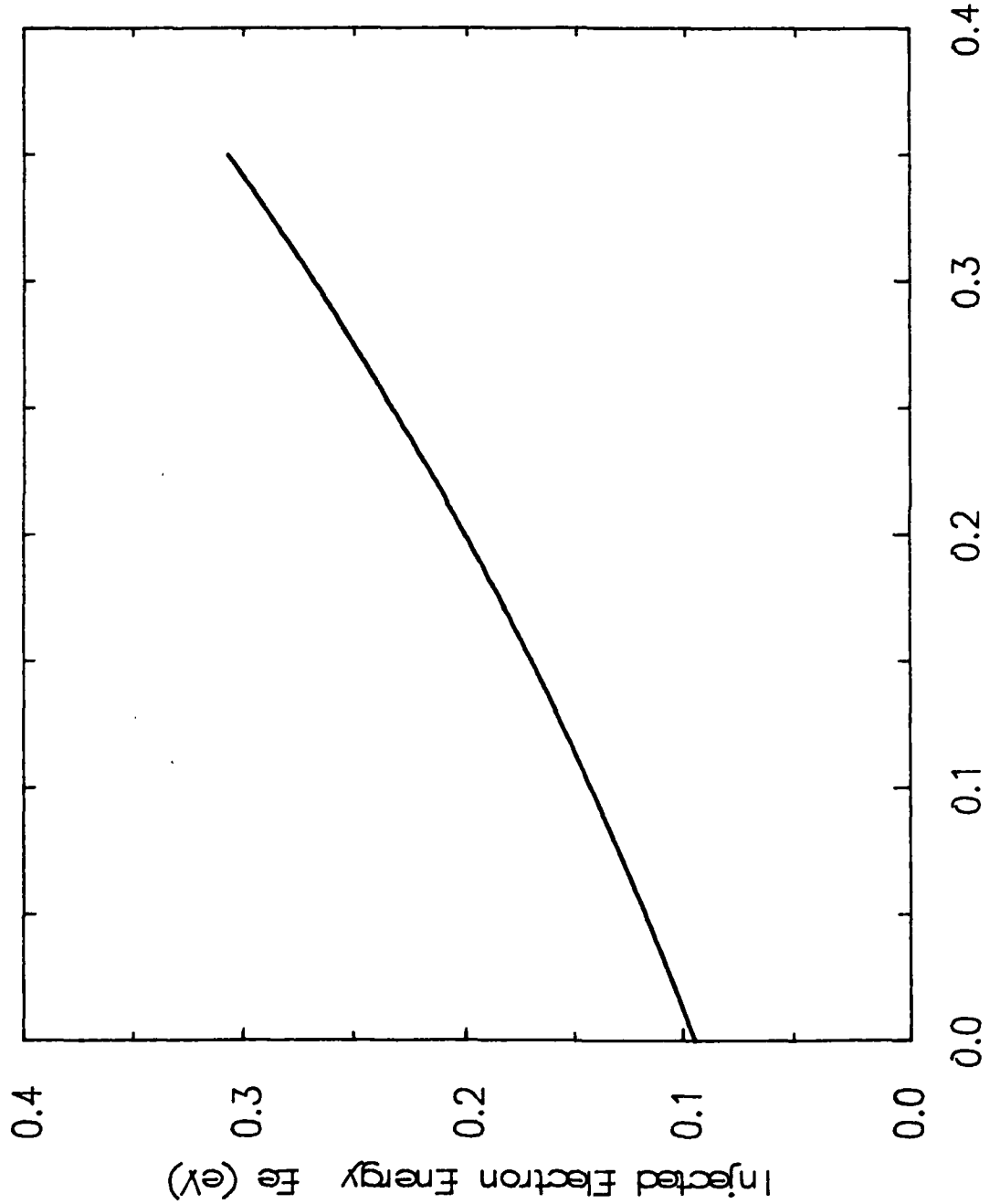

Fig. 2b. Injected electron energy vs. applied voltage.

1. Alignment marks and source contact etch

The process began by coating the GaAs chips (about 10 mm x 10 mm) with AZ4110 resist (5000 rpm spin). After the resist was patterned, GaAs layers were etched about 0.8 μm down to the n^+ source contact layer in H_3PO_4:H_20_2:H_2O = 3:1:50. This etch solution having a relatively low etch rate of 60 nm/min generates smooth etched surface and 45^0 sloping sidewalls. The etched depth was monitored by an Alpha-step profilometer. The alignment marks for the subsequent levels were also defined in this step.

2. Active area definition

This step defines the active area of the device by boron (B_{11}^+) implantation to confine the device current to the drain finger region and to insulate the drain bar source contact cross over as shown in Figure 3. A 2 μm thick resist, AZ4210 (5000 rpm spin), was used to mask the implant. An overhanging resist profile generated by a chlorobenzene pre-develop soak was used to minimize the formation of an ion-hardened resist film around the periphery of the resist mask which can prove difficult to remove. A three energy implant schedule was chosen, 40 keV, 90 keV and 130 keV with three doses of $1.0 \times 10^{13} cm^{-2}$.

3. Drain finger and source contact definition

The 0.6 μm wide drain fingers were patterned in thinned AZ4110 resist (AZ4110:AZ thinner = 3:1, 3000 rpm spin). To obtain the required lift-off profile, a four minute, 30°C chlorobenzene soak

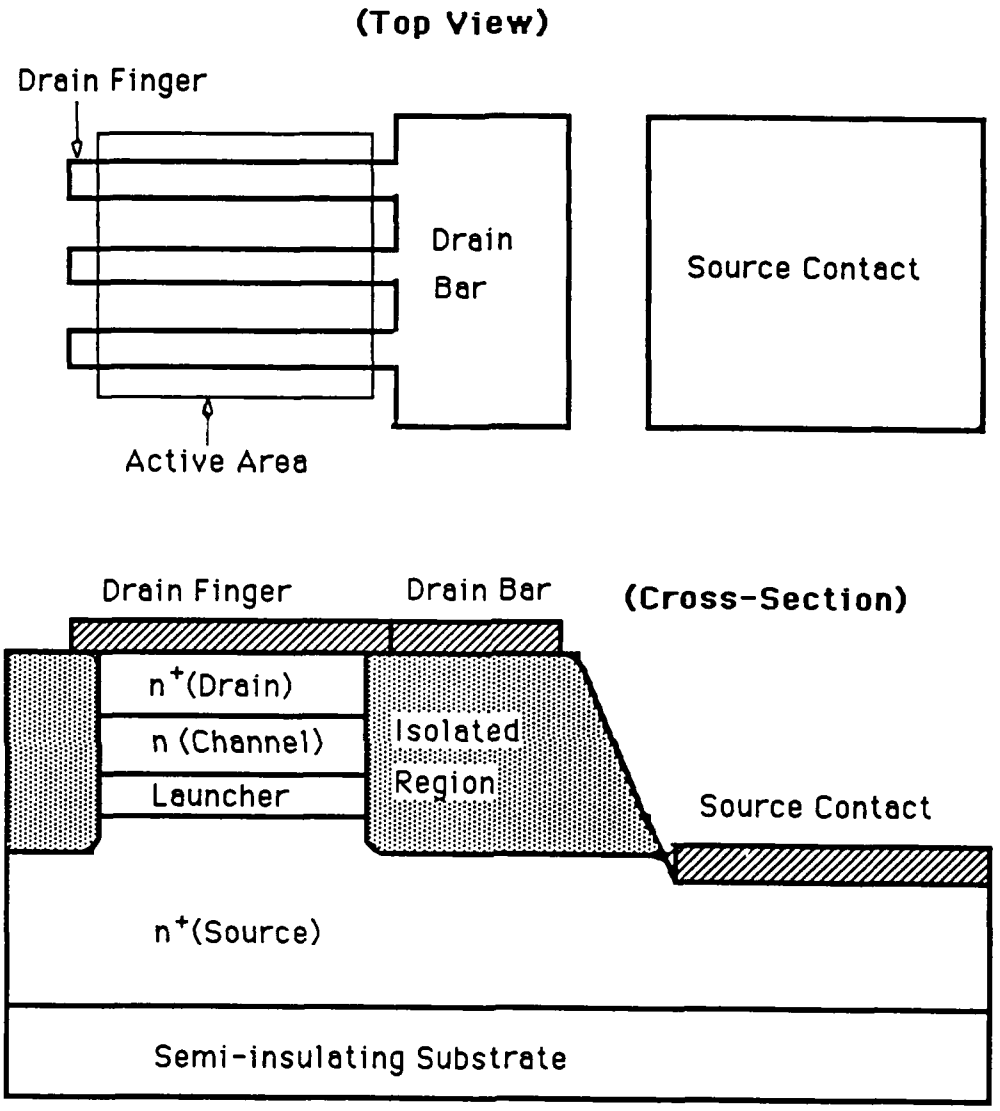

Fig. 3 Schematic illustration of drain bar-source contact crossover isolation by boron implantation.

was utilized. Prior to deposition of the ohmic metallization, a then second O_2 plasma ash was performed to remove any residual resist film from the developed openings, followed by a 15 second $(NH_4OH:H_2O_2:H_2O):H_2O$ = (1:2:1):400 etch to remove the surface oxide. The source and drain ohmic metallizations were performed simultaneously by evaporation of AuGe/Ni/Ag/Au/Ti = 80 nm/9 nm/101 nm/100 nm/50 nm and by lift-off. The drain finger posts were formed by Ar ion milling in an O_2 ambient. The capping layer of Ti acted as a milling mask. Milling was performed to a depth of 0.3 μm, which was monitored by use of an Alpha-step profilometer and a scanning electron microscopy (SEM).

4. Channel undercut etch

Prior to channel undercut etch, the drain bar was protected with resist (AZ4110) from being etched with the undercut profile at its edges. An ammonia-based etch, $(NH_4OH:H_2O_2:H_2O):H_2O$ = (2:1:100):1, was used for the channel undercut etch. The etching rate is 110 nm/min. The etched depth (130 nm) and the undercut profile were carefully monitored by an Alpha-step profilometer and an SEM. The resulting bottom GaAs width, that is, the channel width, was 0.6 μm.

Then, the Ti (TiO_2) milling mask was removed in $HF:H_2O$ = 1:10 leaving a clean chip surface ready for the ohmic alloy cycle. The alloy cycle was performed for 110 seconds in a 600°C furnace in a dry nitrogen ambient with maximum sample temperature of 440°C.

5. Isolation implantation

As the devices were intended only for dc measurement, we skipped over a mesa isolation step. The isolation among the source, drain and gate pads was done by boron implantation. A two energy implant schedule (40 keV, 1.0 x $10^{13}cm^{-2}$ and 100 keV, 1.0 x $10^{13}cm^{-2}$) was chosen. A thick resist, AZ4330 (3500 rpm spin), with chlorobenzene pre-develop soak was used to mask this implant. After the implant and resist strip in acetone, residual resist was removed in a one minute oxygen plasma etch.

6. Gate metallization

The gate metal (Ti, 130 nm in thickness) was deposited onto the sidewall of the n-channel and partly on the launcher and the drain n^+ layer by dual angle evaporation by taking advantage of the undercut profile. The angle (17^o) was determined based on knowledge of undercut profile (SEM photographs) and desired position of the gate. After evaporation, the active area and gate pad region was protected with resist (AZ4110, 4000 rpm spin) and the unwanted Ti was removed in $HF:H_2O$ = 1:10.

7. Drain and gate pad metallization

The final step of the process was to define the drain and gate pads by liftoff using AZ4210 resist (5000 rpm spin) with chlorobenzene pre-develop soak. The pad metallization consisted of 150 nm Ti and 300 nm Au.

2.2.3 Device Results and Discussion

The dc electrical characteristics of the fabricated devices were measured at room temperature and also at liquid nitrogen temperature. The I-V characteristics of VFETs with and without launcher are shown in Figures 4a-4d. The source parasitic resistance (R_S) determined by end resistance method was successfully reduced to 10 Ω (0.36 Ωmm), which is comparable to the best values of lateral type GaAs MESFETs or MODFETs. Unfortunately, the obtained channel width (0.6 μm) was too large to show good pinch-off characteristics. The turn on drain voltage was much larger than the launcher barrier height, mainly due to poor (nonlinear) I-V characteristics of the top drain ohmic contact. The gate voltage dependence of the I-V characteristics of VFETs with the launcher was very unusual. In the small negative gate voltage region, the drain current could be hardly modulated by the gate voltage. We will discuss later the possible causes for this strange characteristic. In the small drain voltage region, the drain currents increases with increasing the gate voltage in the negative direction. This is due to an increase in the gate-to-drain reverse leakage current.

The transconductance values are plotted as a function of the gate voltage for both types of devices in Figure 5. The transconductance of a conventional VFET without launcher normally decreased with increasing the gate voltage in the negative direction. On the contrary, the transconductance of a VFET with launcher increased with increasing the negative gate voltage, and the values

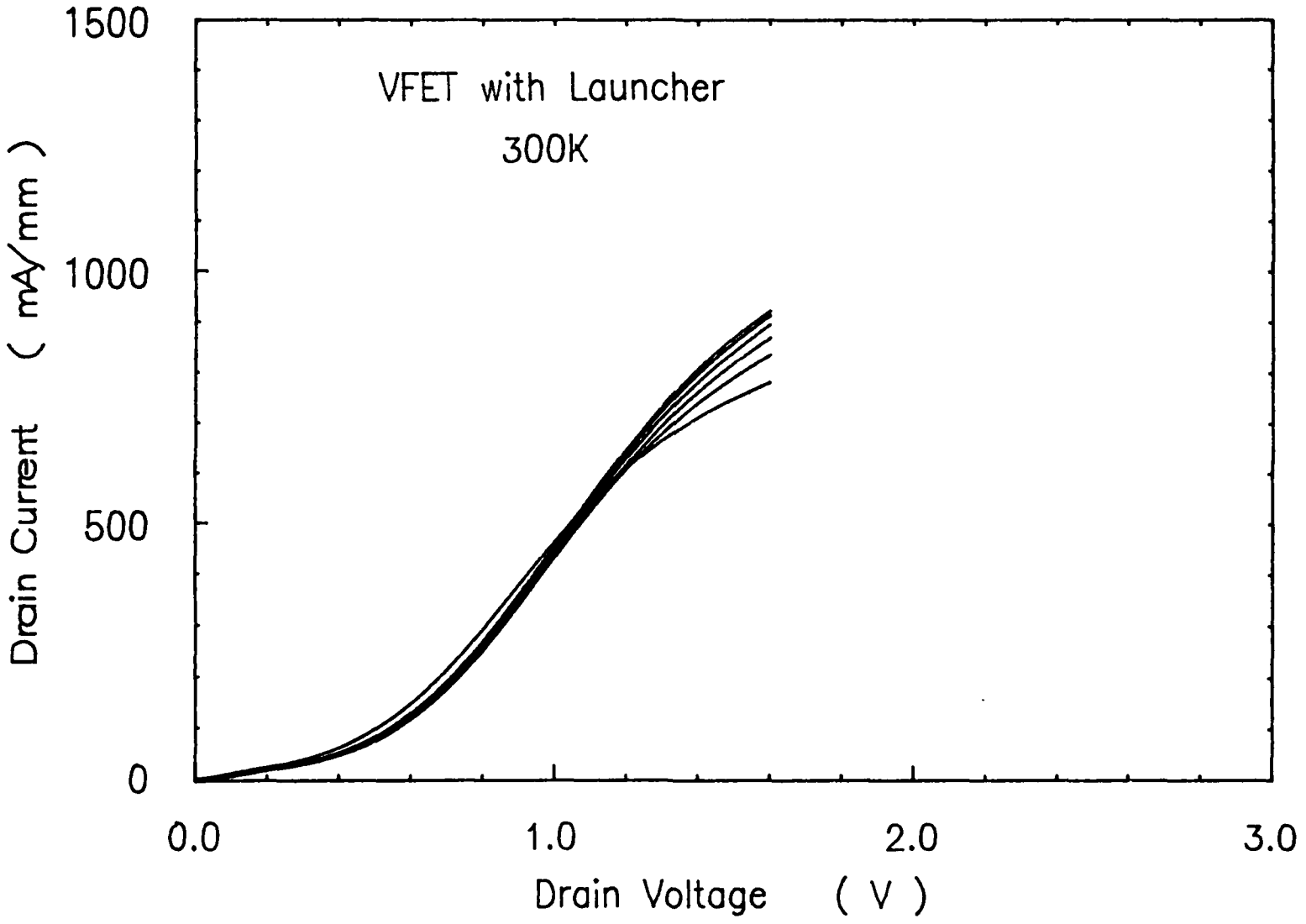

Fig. 4a I–V characteristics of a VFET with launcher measured at room temperature. V_{gs} = 0.0 ~ −5.0 V, −1.0 V step.

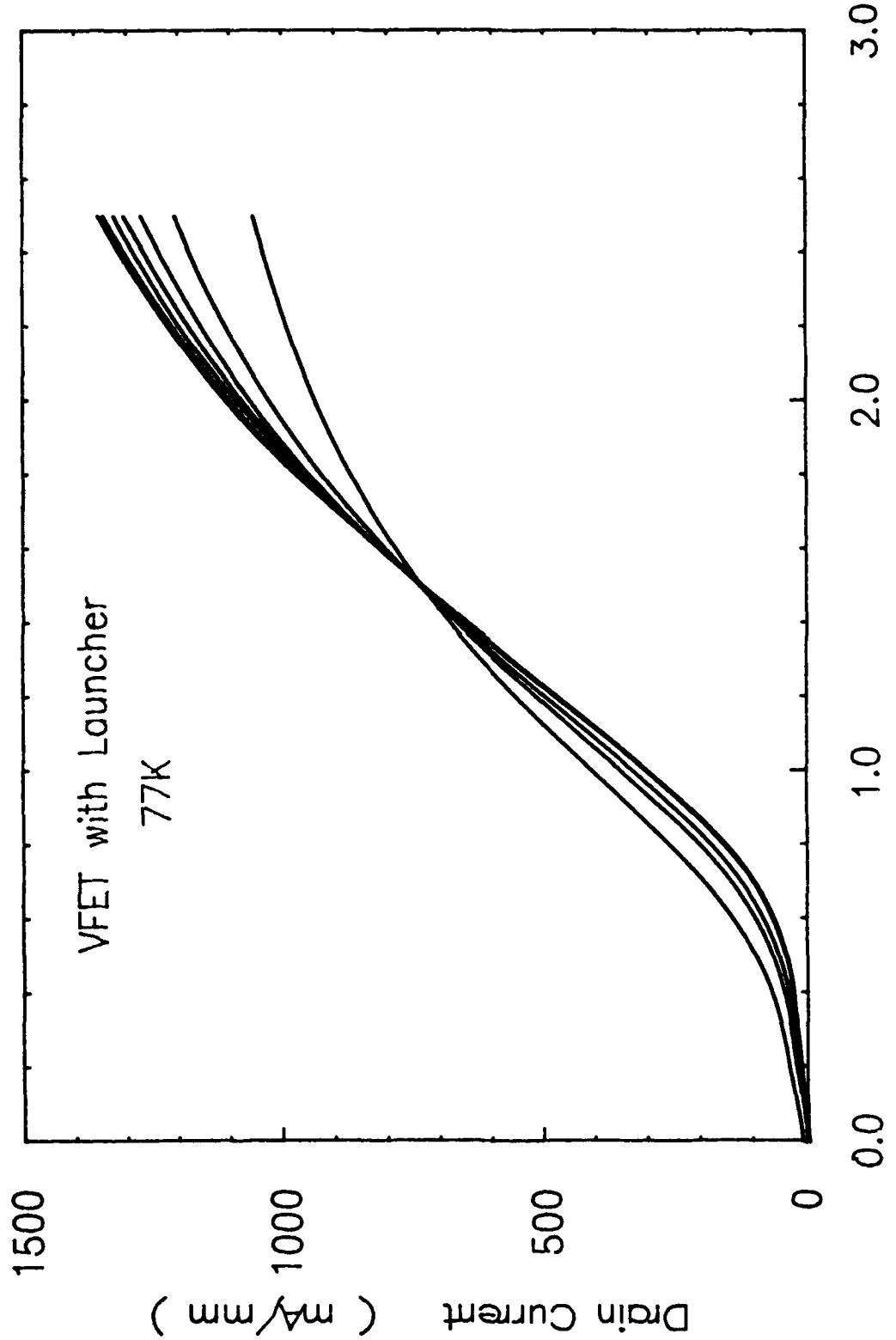

Fig. 4b I-V characteristics of a VFET with launcher measured at 77 K.
V_{gs} = −0.5 ~ −6.5 V, −1.0 V step.

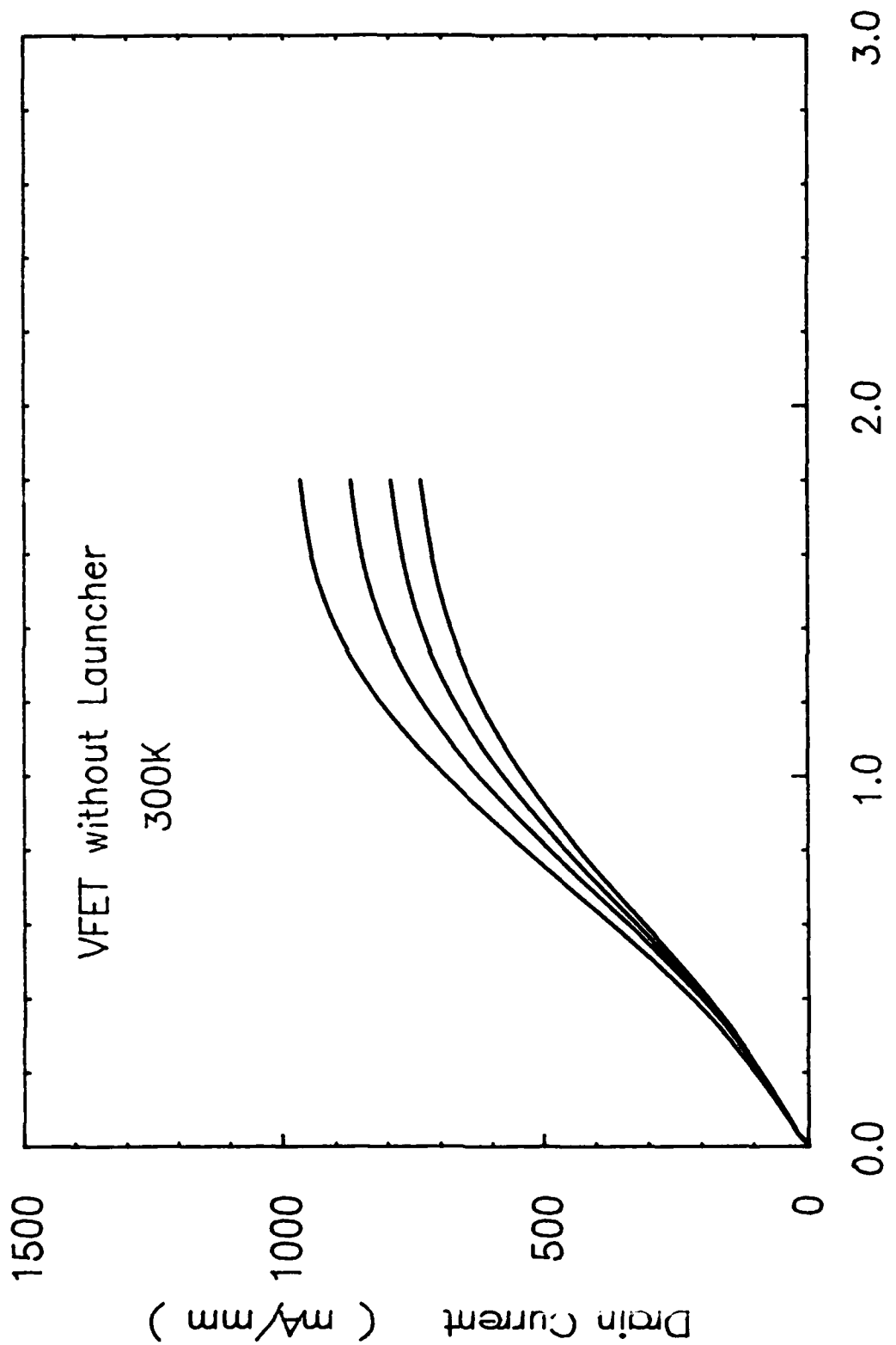

Fig. 4c I–V characteristics of a VFET without launcher measured at room temperature. V_{gs} = 0.0 ~ −3.0 V, −1.0 V step

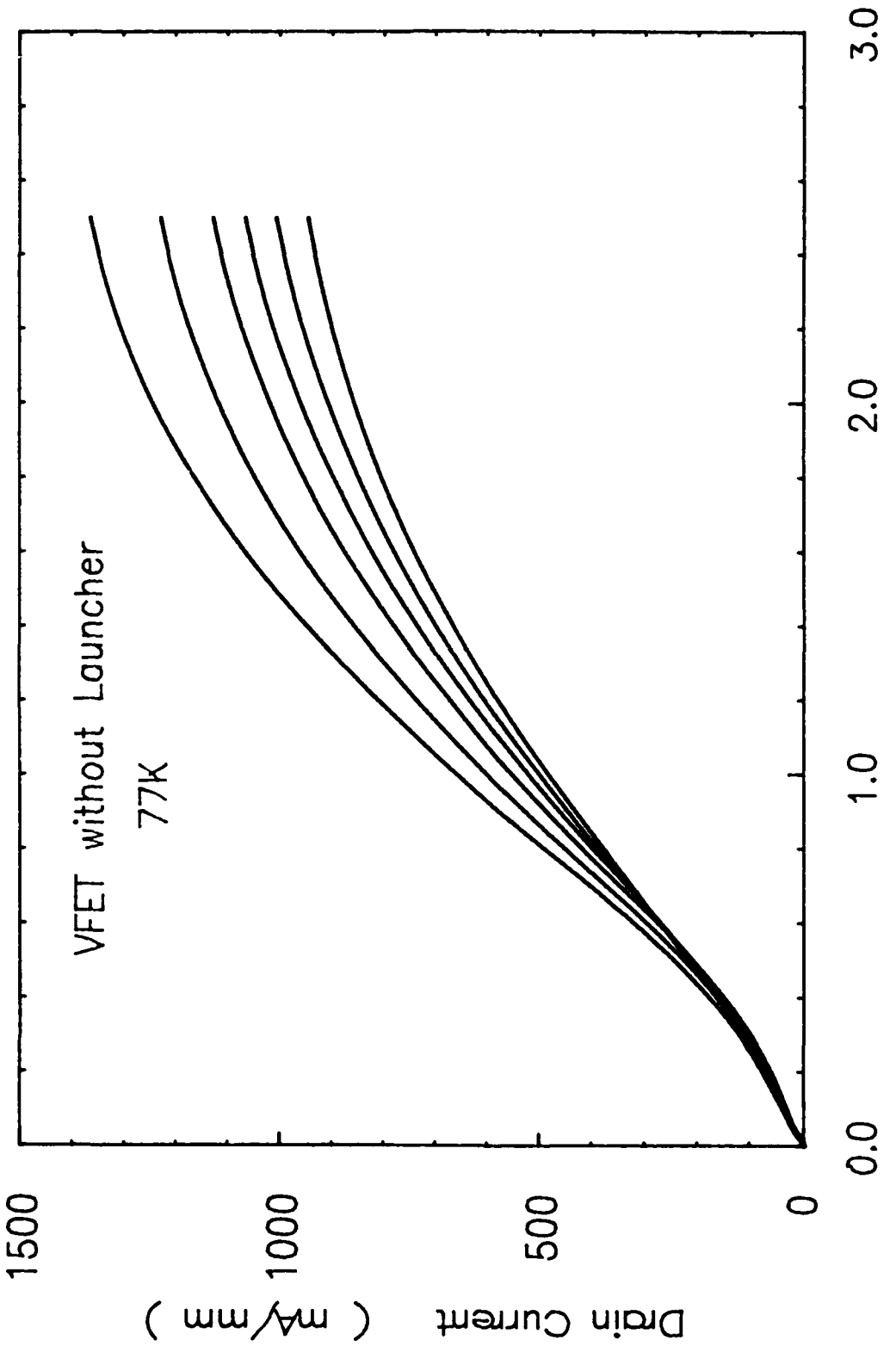

Fig. 4d I–V characteristics of a VFET without launcher measured at 77 K.
V_{gs} = 0.0 ~ −5.0 V, −1.0 V step.

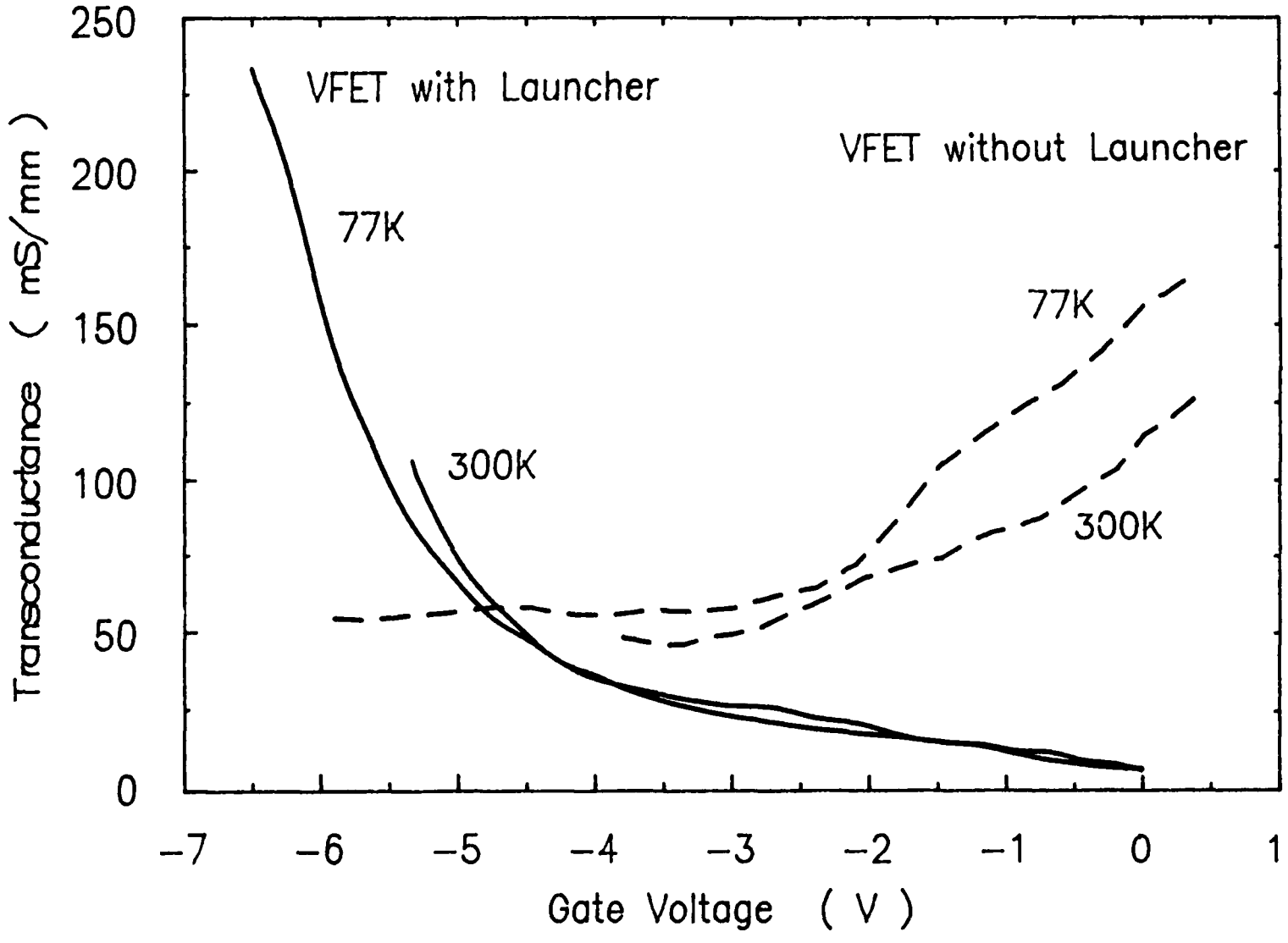

Fig. 5 Transconductance versus gate voltage. V_{ds} = 2.5 V (77 K) and 1.6 V (300 K) for VFET with launcher. V_{ds} = 2.5 V (77K) and 1.8 V (30C K) for VFET without launcher.

were very small in the region of small negative gate voltage. The reason for this unusual characteristic can be attributed to the launcher as follows. The device is composed of a launcher and a FET in series. In the large current region (drain current I_d > 1300 mA/mm for the I-V characteristics at 77°K), that is, in the small negative gate voltage region, the drain current is determined dominantly not by the channel but by the launcher. The current density is so large (> 4 x $10^5 A/cm^2$) that the current is limited by the carrier density and thermal electron velocity in the source n^+ layer and space charge effects in the undoped and p^+ layers of the launcher. Since the launcher acts as a large series resistance, it suppresses the extrinsic transconductance. These poor characteristics could be improved by using a better launcher which allows larger current density.

However, in the relatively large negative gate voltage region, the transconductance values were 4-5 times as large as those of the conventional VFET at the same gate voltage. This is because the drain current is much smaller than the maximum launcher current and it is determined dominately by the channel instead of the launcher. The drain current is effectively modulated by the gate voltage. The maximum transconductance (234 mS/mm) obtained at 77°K in the VFET with the launcher, which was unfortunately limited by the breakdown voltage of the gate, was larger than the maximum value (165 mS/mm) in the conventional device. It should be noted that cooling the device to cryogenic temperature is not essential, but it only increases the breakdown voltage. Optimization of doping

densities of the launcher and channel are required for improvement in the I-V characteristics.

The devices have a relatively large channel width of 0.6 μm. This is the main cause for non-pinch off characteristics and poor drain current saturation characteristics. The pinch off voltage (V_p) for the one dimensional model is given by

$$V_p = (qN_D/2e_s)(W/2)^2 \ ,$$

where N_D is the doping density of the channel and (W/2) is the half channel width. With 1 x $10^{17}cm^{-3}$ for N_D and 0.3 μm for (W/2), V_p is estimated to be 6.5 V. However, the experimental pinch off voltage was much larger than the estimated value. This is because the aspect ratio of $L_g/(W/2)$ (= 0.43), the ratio of the gate length to the half channel width, is less than 1. Therefore, the depletion layer shape is almost circular, instead of flat, as assumed in the one dimensional model. The pinch off voltage increases due to this two dimensional effect. This low aspect ratio also results in a poor drain current saturation characteristics. The drain field has a considerable influence on the carrier distribution in the entire channel, leading to an increase in the output conductance. In order to suppress these two dimensional effects, we have to reduce the channel width down to 0.3 μm at least and increase the aspect ratio of $L_g(W/2)$.

The average electron velocity (v_{av}) in the channel was evaluated from the relationship between the drain current (I_d)

and the gate to channel voltage (V_{gc}). By using the saturation velocity model for the MESFET, the drain current is given by

$$I_d = -v_{av}(2e_s qN_D V_{gc})^{1/2} Z + qnv_{av}(W/2)Z,$$

where Z is the gate width. The gate to channel voltage is given by

$$V_{gc} = V_{gs} - V_{bi} - I_d R_s - V_1,$$

where V_{bi} is the built in voltage assumed to be 0.7 V and V_1 is the voltage drop in the launcher.

The drain current values measured at 77°K at a fixed intrinsic drain voltage (voltage drop through the channel) of 0.25 V are plotted in Figure 6 as a function of square root of the gate to channel voltage taking into account the voltage drop in the launcher (0.2-0.34 V). From the slopes, average velocity values of 6.4 x 10^7cm/s and 3.3 x 10^7cm/s were obtained for the VFET with the launcher and for the conventional VFET, respectively. The enhancement of the average velocity by a factor of about 2 might best be attributed to hot electron injection into the channel.

The current gain cut off frequency f_T of the intrinsic FET is approximately given by

$$f_T = v_{av}/(2\pi L_g).$$

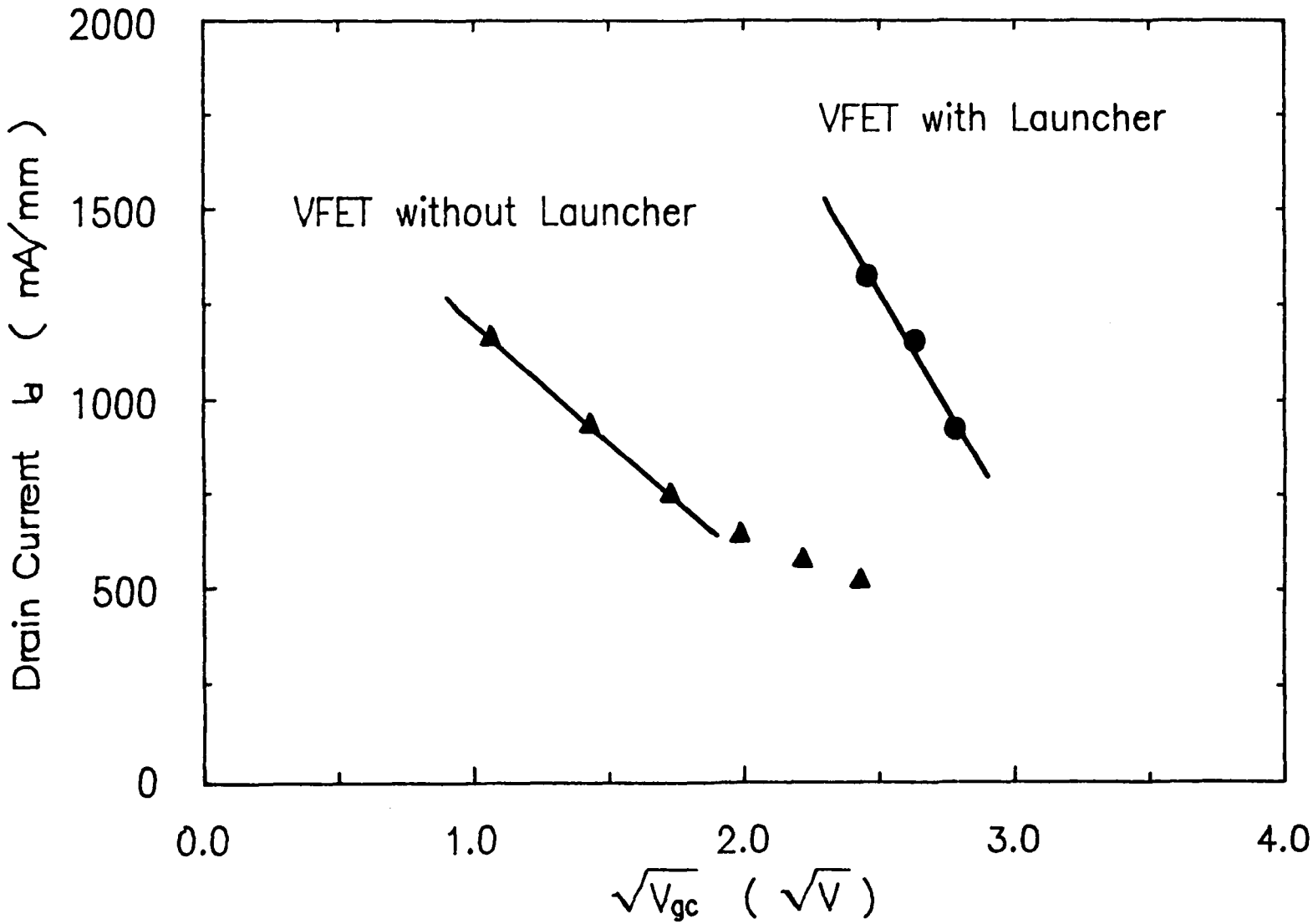

Fig. 6 Drain current at a fixed intrinsic drain voltage of 0.25 V versus square root of the gate to channel voltage.

With 6.4 x 10^7cm/s for v_{av} and 0.13 μm for the gate length L_g, we can estimate a very large f_T of 780 GHz. This value is about four times as large as the best reported values of short gate length (0.1 m) MODFETs. In order to realize this superior high frequency performance, we have to reduce the parasitic gate-to-source and gate-to-drain capacitances, which might be larger than the intrinsic gate capacitance for the present device structure. This reduction can be done by, for instance, sophisticated air bridge and self aligned technology.

2.3 Hot electron Spectrometer

2.3.1 Device Structure and Fabrication

The epitaxial layers were grown by MBE on a semi-insulating GaAs substrate. A schematic layer structure is shown in Figure 7a. Both launcher and analyzer were composed of n^+-i-p^+-i-n^+ PDBs. The zero bias barrier height of the analyzer was designed to be larger than that of the launcher. The doping density and thickness of the channel n layer were 2 x 10^{16}cm^{-3} and 130 nm, respectively. Though a very thin drain n^+ layer is desired for diminishing the energy loss by scattering with coupled plasmon optical phonon modes in this layer, the reduction of the thickness is limited for technical reasons to put the drain metal precisely on it. It is also limited by the increase in its sheet resistance. Therefore, a thickness of 40 nm with 2 x 10^{18}cm^{-3} doping density was chosen for the drain n^+ layer.

n^+	3×10^{18} cm^{-3}	100 nm	
n^+	1×10^{18} cm^{-3}	100 nm	
undoped		30 nm	
p^+	2×10^{18} cm^{-3}	7 nm	Analyzer
undoped		30 nm	
n^+	2×10^{18} cm^{-3}	40 nm	Drain
n	2×10^{16} cm^{-3}	130 nm	Channel
n^+	2×10^{18} cm^{-3}	16 nm	
undoped		3 nm	
p^+	2×10^{18} cm^{-3}	8 nm	Launcher
undoped		10 nm	
n^+	4×10^{17} cm^{-3}	300 nm	
n^+	3×10^{18} cm^{-3}	1000 nm	Source
Semi-insulating Substrate			

Fig. 7a Schematic cross-section of MBE layer structure for fabricating hot-electron spectrometers.

The device structure is schematically shown in Figure 7b. The device was constructed of a non-gated VFET and an analyzer on it. Self aligned drain fabrication technology was used to minimize the drain parasitic resistance. The fabrication steps were very similar to those of VFETs as described in section 2.2.2. The active area (6 μm x 12 μm) was defined by selective isolation implantation of boron ions. The analyzer ohmic fingers composed of AuGe/Ni/Ag/Au/Ti (0.6 μm wide with 2 μm periodicity) were formed by lift off technique. Then GaAs layers were milled in Ar + O_2 to a depth of 150 nm by using the analyzer fingers as a protection mask, followed by wet chemical etching (120 nm in depth) with undercut in solution of $NH_4OH:H_2O_2:H_2O$. The resulting bottom GaAs width was the same or slightly smaller than the top ohmic metal width. Next, Ti drain metal (100 nm in thickness) was deposited on the drain n^+ layer by normal angle evaporation by using the overhang structure. The resulting lateral spacing between the analyzer and drain metal was less than 0.1 μm. Consequently, the total drain n^+ layer area was 72 μm^2 and the total analyzer area was about 20 μm^2. Schottky contact drain was chosen instead of ohmic contact in order to avoid the metal penetration into the channel. This nonlinear drain required some sophisticated measurement technique as explained in the next section.

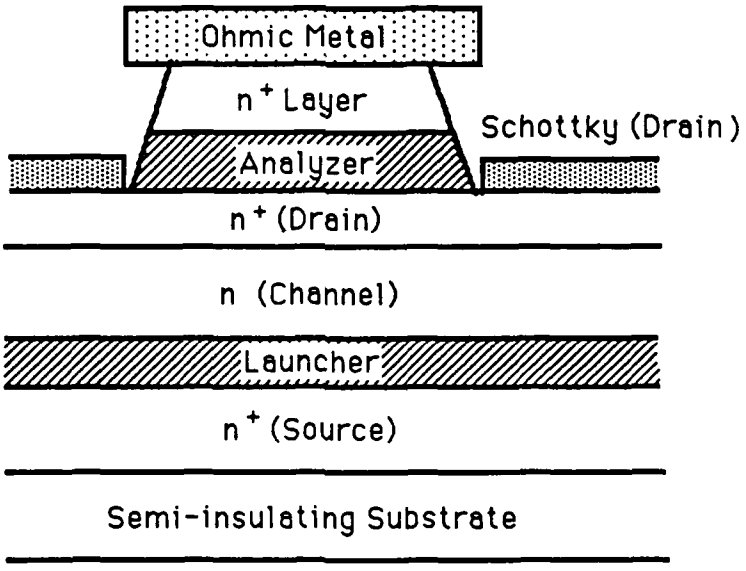

Fig. 7b Schematic cross-section of a single post of a multi-finger hot-electron spectrometer.

2.3.2 Results and Discussion

The electrical measurements were performed at 77°K and in the dark. The analyzer current (I_a) was measured by varying the analyzer voltage (V_a) at a fixed drain current (I_d) instead of a fixed source current. The distribution, $n(P_n)$, of electrons having particular values of momentum normal to the analyzer, P_n, is determined by

$$n(P_n) = dI_a/dV_{ad}^{i},$$

where V_{ad}^{i} is the intrinsic voltage drop of the analyzer. This value is given by

$$V_{ad}^{i} = V_a - V_d - I_aR_a + V_{dp},$$

where R_a is the parasitic resistance of the analyzer and V_{dp} is the voltage drop of the drain including the n^+ layer, the Schottky junction and the metal. As the value of V_{dp} is kept constant independent of V_a for each I_d, this measurement technique can eliminate the effect of nonlinear drain characteristics. The barrier heights of the launcher and analyzer were determined by characteristics of I_a vs. V_d and I_a vs. $(V_a - V_d)$ at zero drain current, respectively.

The hot electron spectra for various drain currents are shown in Figure 8. In the forward current region, where electrons flow

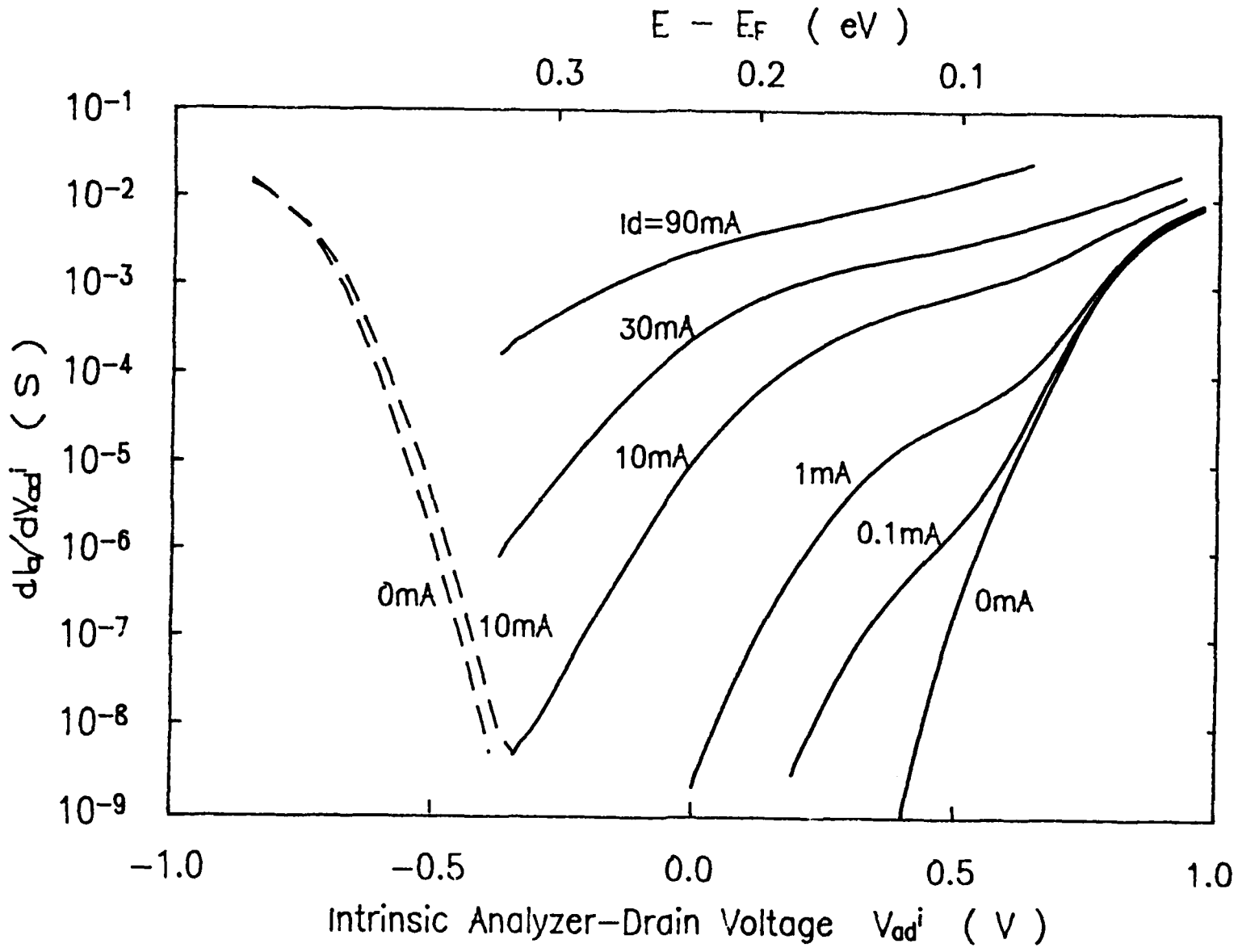

Fig. 8 Hot−electron spectra for various drain currents (solid lines). The broken lines show the reverse characteristics representing distibution of thermal equilibrium electrons.

from the drain to analyzer, the differential value of $dI_a/dV_{ad}{}^i$, that is, the distribution of electrons arriving at the drain through the channel, dramatically increased with the drain current. On the contrary, in the reverse current region, the differential value representing the distribution of the steady state electrons in the cap n^+ layer slightly changed with the drain current. The injected electron energies estimated from the I-V characteristics of the launcher were 0.18 eV at I_d = 0.1 mA and 0.24 eV at I_d = 90 mA, respectively. Although there was no evidence of ballistic transport through the channel, it was confirmed that some electrons have large energy and the distribution diverges from the steady state one. This indicates that the initial injected hot electrons lose some energy by scattering in the channel, but still they are hot. It should be noted that electrons are also scattered in the drain n^+ layer, because the thickness is a little larger than the mean free path. Assuming that the mean free path is 25 nm, 80% of the electrons scattered in this region. For improvement in the sensitivity, it is necessary to reduce the drain thickness.

The effective electron temperature (T_e) was determined from the slope of the curve in Figure 8. The electron temperatures estimated at a fixed $V_{ad}{}^i$ of 0.25 V are plotted as a function of the drain current in Figure 9. In this figure, the lattice temperatures (T_i) determined from the reverse current region by the same method are also plotted. The electron temperature increased with the drain current and exceeded 1000°K at 30 mA ($8 \times 10^4 A/cm^2$) of I_d. This is because the injected energy, the acceleration by the electric field in

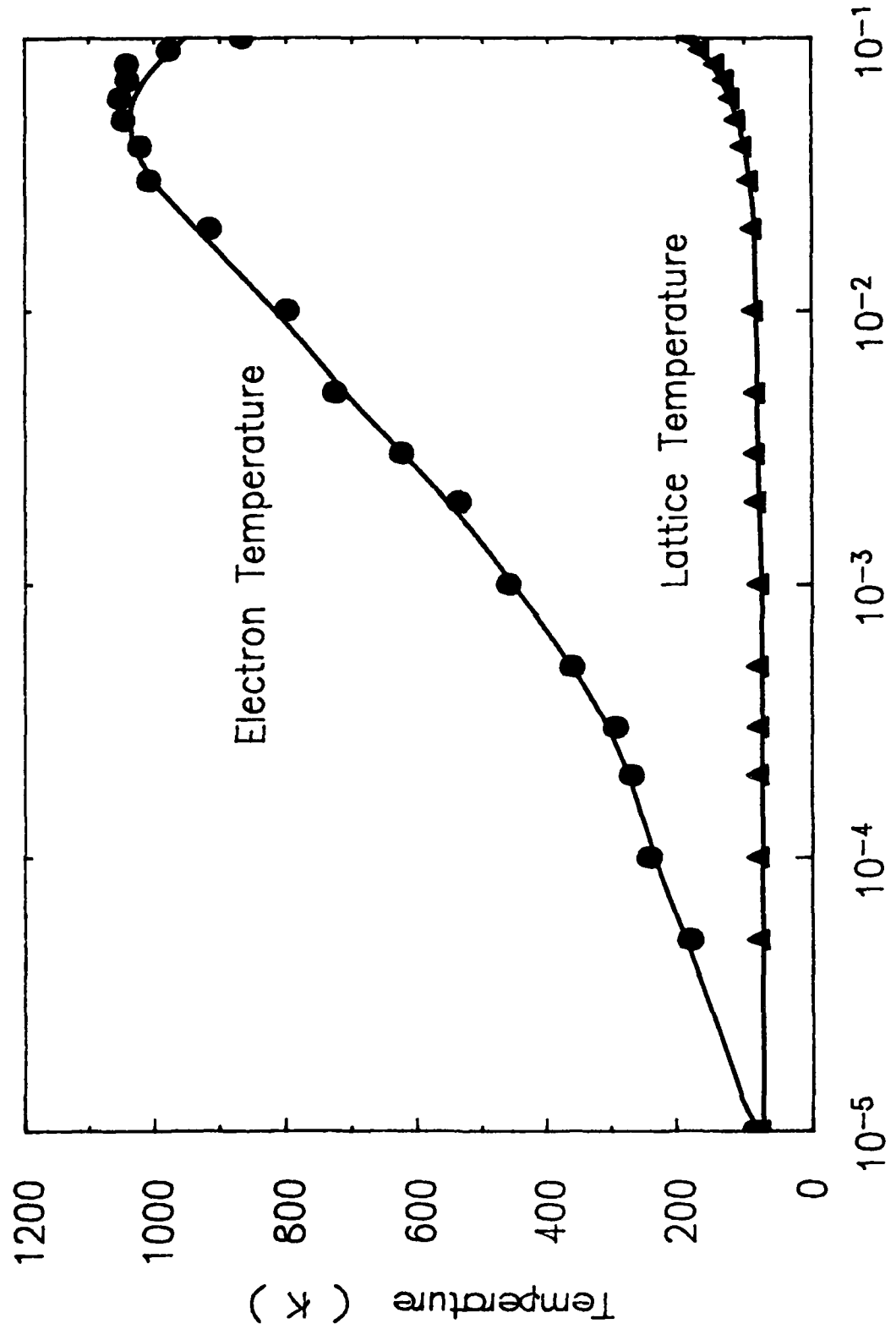

Fig. 9 Electron temperature and lattice temperature versus drain current.

the channel, and the ratio of the injected hot electrons to the thermal equilibrium electrons are increased with the drain current. In contrast, the lattice temperature was kept low as 90°K even at I_d = 30 mA. At 100 mA of I_d, the lattice temperature increased up to 180°K by current heating effects, and the electron temperature decreased to 900°K.

At I_d = 60 mA, the analyzer current at 0.5 V of $V_{ad}{}^i$, which represents the contribution to the total current of hot electrons having energy larger than 0.1 eV above the steady state Fermi energy, was 2 mA. Assuming that the mean free path in the drain n^+ layer is 25 nm and taking into account of the area ratio of the analyzer to the drain n^+ layer, it is deduced that 60% of electrons have energies larger than 0.1 eV at the drain edge of the channel. On the assumption that the electron mobility is 1000 cm^2/Vs, the voltage drop in the channel is estimated to be only 0.03 V. Therefore, the dominant cause of the energetic electrons is the hot electron injection.

One of the disadvantages of PDB analyzer is poor energy resolution, because the barrier height fluctuates spatially due to the discreteness of the acceptors. Another reason is that electron transmission coefficient through the barrier gradually changes with the energy due to quantum mechanical reflection and tunneling. The resolution can be experimentally estimated from the temperature dependence of the barrier height. Assuming that the barrier height distribution function is a Gaussian with a mean value of E_{av} and standard deviation of s, the effective barrier height (E_{eff})

determined from I-V characteristics decreases with decreasing temperature by

$$E_{eff} = E_{av} - s^2/2kT.$$

As the effective barrier heights of the analyzer were 0.40 eV at 300°K and 0.23 eV at 77°K, the value of the standard deviation was estimated to be 55 meV. This value is small enough to probe the ballistic peak, if the peak exists.

2.4 Conclusions

The advantage of hot electron injection into an FET channel has been experimentally demonstrated. A VFET with rapid acceleration of electrons in the launcher had the maximum transconductance of 234 mS/mm and the average electron velocity of 6.4 x 10^7cm/s. These values are 1.4 and 1.9 times as large as those of a conventional VFET with gradual acceleration through the channel. An unusual characteristic in the large current region is due to the current limitation in the launcher and it could be improved by optimization of layer structure. In order to obtain the good pinch off characteristics and to reduce the output conductance, we have to reduce the channel width. The intrinsic current gain cut off frequency is estimated to be 780 GHz with the above value of the average electron velocity.

Electron energy distribution in a VFET with launcher have been successfully measured at 77°K by fabricating a hot electron spectrometer. Although there is no evidence of ballistic transport through the channel, the spectra show that electrons arriving at the

drain have large energy compared with the thermal energy. The effective electron temperature increases over 1000°K with the drain current. The hot electrons, dominately created by the launcher, contribute to enhance the average electron velocity in the channel leading to improvement in high frequency performance of VFETs.

I.E. CONCLUSIONS AND RECOMMENDATIONS FOR PART I

It is concluded that the source-up configuration has too high a source resistance, and source-down configurations do not. It is also concluded that .5 μm drift space is too long for maintaining average transit velocity at or above 5 x 10^7 cm/s. .13 μm drift space yielded high electron velocity, but could not be pinched off due to channel thickness (.6 μm). A compromise drift distance between these values would be optimum. It is further concluded that planar-doped barriers are the most effective ballistic electron launchers, and that O bias barrier heights in the range of .2 - .25V are optimum, in order not to have electrons slowing down due to their transfer to upper valleys.

Although not yet certain, until microwave devices are made and tested, it now appears from DC data that the short devices (.13 μm devices tested) yield at least 3 x 10^7 cm/s average electron transit velocity with no ballistic electron launcher, and at least 6 x 10^7 cm/s when such launchers are used.

It is recommended that planar doped barriers be placed in devices with appropriate channel/gate aspect ratios, such as

permeable base transistors, in order to have fast electrons in addition to being able to pinchoff the device current. Such devices, will have f_t (unity current gain frequency) well over 100 GHz, rather than the 40 GHz of present PBT's.

F. ACKNOWLEDGEMENTS

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REFERENCES

1. J.M. Shannon, Appl. Phys. Lett., 35 (1) 63-65 (July 1979).

2. R.J. Malik, K. Board, C.E.C. Wood, L.F. Eastman, T.R. AuCoin and R.L. Ross, Electron. Lett., 16 (22) 836-838 (oct. 1980.

3. P.J. Tasker, private communication.

4. U. Mishra, E. Kohn and L.F. Eastman, Proc. 1982 IEDM, pp. 594-597 (Dec. 1982).

5. C.O. Bozler and G.D. Alley, IEEE Trans. Elec. Dev., ED-27 (6) 1128-1140 (June 1980).

6. M.A. Hollis, K.B. Nichols, R.A. Murphy, R.P. Gale, S. Rabe, W.J. Piacentini, C.O. Bozler and P.M. Smith, Proc. 1985 IEDM, pp. 102-105 (Dec. 1985).

7. K. Nagata, O. Nakajima, T. Nittono, H. Ito and T. Ishibashi, Elec. Lett., 23 (11) 566-568 (May 1987).

8. A. Al-Omar and J.P. Krusius, IEEE Elec. Dev. Lett., 9 (2) 81-83 (Feb. 1988).

TECHNICAL RESULTS - PART II

II.A. PROGRAM OBJECTIVE FOR PART II

The objective of this contract is to study layer stability and contact formation in GaAs structures. The work has emphasized two directions:

1. stable metallization using deposited Si, Co and Ge on GaAs
2. contact formation via diffusion (a-Si/GaAs) and heterojunction structures (Ge/GaAs).

II.B. SUMMARY FOR PART II

1. The Poly-Si Contact to GaAs

The latest contact measurements have shown that As doped polycrystalline-Si (9at%) also produces an ohmic contact to GaAs (10^{-4}ohm.cm^2) if annealed at 1000^{o}C. High resolution TEM has found a layer of non-epitaxial material at the interface. The ohmic properties of both the P and As-Si samples may, for example, be associated with a Ga accumulation at the interface, rather than anything related to P passivation of interfacial states, phase formation or heavy substrate doping. However, high spatial resolution electron energy loss spectroscopy (SREELS) on thin cross-section samples failed to identify a metallic Ga layer.

2. Co/GaAs

Studies of the Cobalt and GaAs has continued. At temperatures of 500^{o}C, Cobalt is completely consumed in a solid phase reaction to

form a single compound. Energy Dispersive Spectroscopy (EDS) and RBS have been used to identify the phase with an average composition of Co_2GaAs. Electron diffraction was used to assess the structure of the Co_2GaAs ternary films. The film was found to consist of two variants of a hexagonal unit cell (NiAs B8) with lattice parameters a_o = 3.41 Å and c_o = 5.32 Å. The orientation relationship with (100) GaAs was determined to be

$$\{111\} \sim'' \{0001\}_{Co_xGaAs}$$

$$<110> \sim'' <2TT_o>_{Co_xGaAs}$$

Below 500°C it was observed that the binary phase CoGa and CoAs were present in a layer adjacent to the surface and above the ternary layer. From a calculated Co-Ga-As phase diagram it can be shown that if a stable ternary compound does not exist, then a reaction mixture of Co and GaAs will come to equilibrium when all the Co has reacted to form equal amounts of CoGa and CoAs. Since the ternary has been shown to exist at 500°C, the simultaneous presence of the binary phases CoGa and CoAs suggests either that the ternary phase Co_2GaAs is a metastable compound or that a kinetic impurity effect plays a role in determining phase formation and sequence. Work is in progress to understand the kinetics of the reaction.

3. Epitaxial Ge/GaAs

Ge deposited on unheated GaAs has been regrown epitaxially at 400°C. The solid phase epitaxy of the Ge takes place only when the GaAs surface is sufficiently clean. We used Ar ion sputtering (3 KeV) in the deposition chamber to obtain adequately clean GaAs surfaces for these experiments. The epitaxial alignment between the Ge and the GaAs was confirmed by channelling measurements and the interface between the Ge and the GaAs as well as the crystallinity of the Ge was studied with cross-sectional transmission electron microscopy. Initial measurements on the electrical behavior of the Ge/GaAs show that the contact formed is ohmic, though of high resistance, as the Ge is undoped. Further efforts are underway to determine the electrical quality of the contact, the influence of the sputter cleaning on the electrical properties, and on doping the Ge either during deposition or by implantation.

II.C. DETAILED RESULTS FOR PART II

1. Phase Formation and Reaction Kinetics in the Thin-Film Co/GaAs System

Solid state reactions between metal thin films and GaAs are of particular importance as stable ohmic and Schottky contacts to GaAs devices. Palmstrom and Morgan have reviewed a number of metallizations for such contacts [1]. Alloyed metallization such as Au-Ge-Ni have been extensively studied. These systems typically exhibit complex phase formation, interface morphology, and growth

kinetics and often involve the liquid phase. For a single metal layer on GaAs, phase formation and reacted layer structure have been studied in significant detail only in a few systems, e.g., Pt/GaAs [2], Pd/GaAs [3], Ni/GaAs [4], and Au/GaAs [5]. The emphasis has been on the electrical properties, specifically the Schottky barrier height, as opposed to the metallurgical aspects of metal/GaAs interactions. Drawing on the extensive results known for metal/Si systems, a good metallization should have a uniform and limited reaction between the metal and semiconductor. It is necessary to have a reaction between the metal and silicon to ensure that there is adhesion and intimate contact. Uniformity is required as deep penetration can start at localized points due to interface instability.

For the Ni/GaAs system, Lahav et al. found that the reaction between Ni and GaAs was controlled by the nucleation of the ternary phase Ni_2GaAs in a large number of reacted islands on the sample surface [6]. A tantalum marker experiment demonstrated that nickel atoms were the diffusing species. Lateral growth of these islands followed. The reaction kinetics for the Pt/GaAs system have been investigated by Kumar [7]. At the endpoint of the reaction, $PtAs_2$ and PtGa were the only products present in the metallic layer. For Pt films thicker than 2000 Å, the initial rapid reaction phase was followed by sharply reduced kinetics; the reaction becomes self-limiting. A continuous layer of $PtAs_2$ was formed at the interface, which limited further outdiffusion of Ga from the GaAs. This report covers initial results on a study of cobalt on (100) GaAs, with the emphasis on fundamental questions of phase formation and growth

kinetics.

Cobalt films 240 nm thick were electron beam deposited in a vacuum of 5 x 10^{-7}Torr on chemically etched and ion beam cleaned (100) semi-insulating GaAs wafers. Annealing was done in a turbomolecular pumped vacuum furnace in a vacuum of 2 x 10^{-7}Torr. Rutherford backscattering spectrometry (RBS) (3 meV He^{++}) was used to analyze composition and thickness of the reacted layers. X-ray diffraction, with a Guinier camera, was used for phase identification.

Interpretation of the RBS spectra of intermetallic compounds consisting of a metal and gallium and/or arsenic is difficult because of the overlapping signals from the three elements. The analysis has been greatly aided by the use of a computer simulation program for RBS spectra developed at Cornell University [8], which enables the contribution of each element to the total spectrum to be displayed separately. Figure 1 shows the RBS spectrum for the as-deposited Co on GaAs, overlayed with the complete simulation. Also shown in Figure 1 are the calculated contributions of each element, Co, Ga, and As to the simulated spectrum. Using the simulation program, the behavior of each element during phase formation can be elucidated.

Isothermal anneals at 400°C were carried out for times from 15 min. to 24 h. Figure 2(a) shows the RBS spectrum for the 1 h anneal. The Co contribution to the RBS spectrum is also shown in Figure 2(a). The step at the back edge of the Co peak shows that part of the Co has reacted with the GaAs. The sharpness of the step indicates that the reacted layer is uniform in composition and the

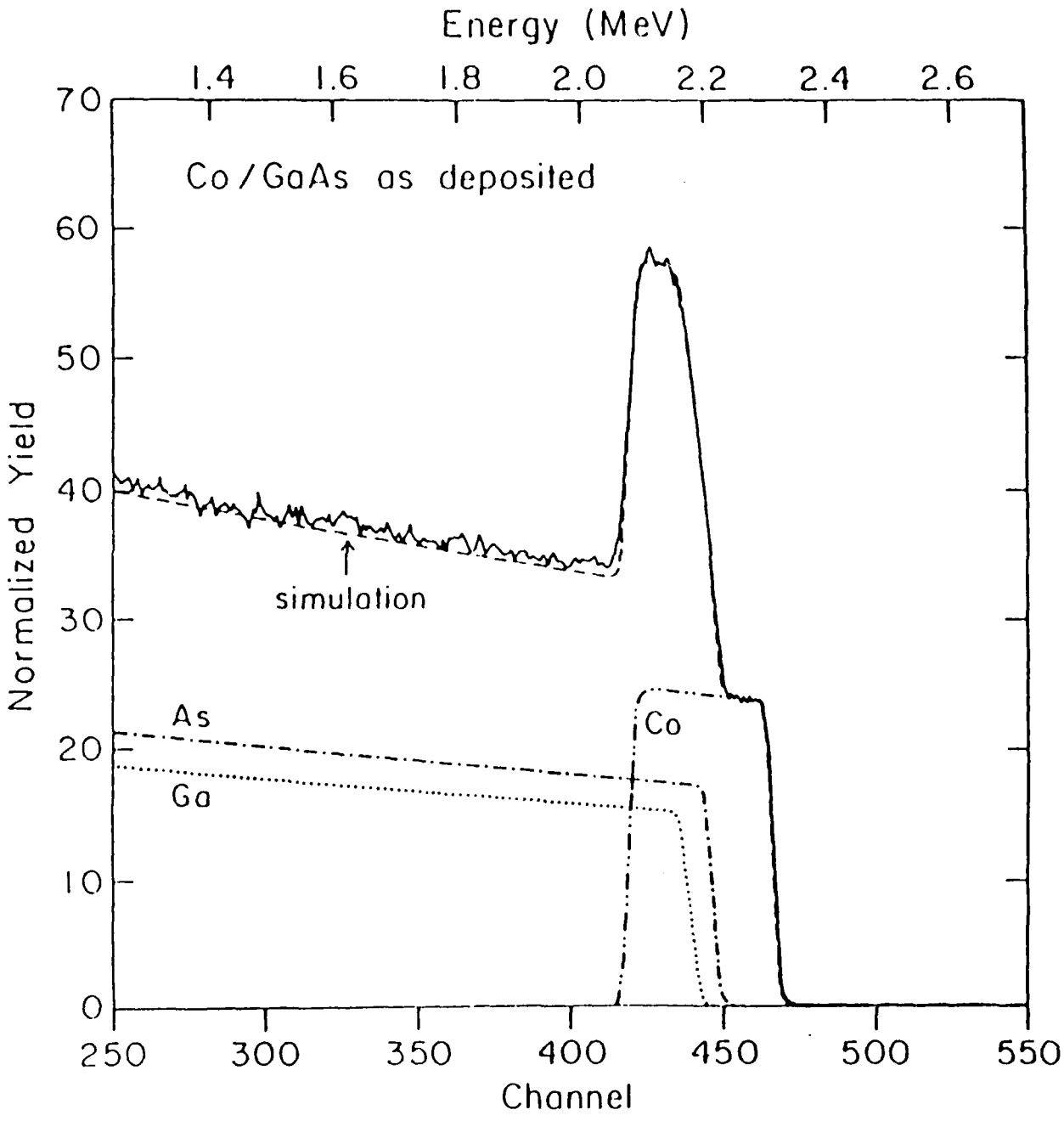

Figure 1. Rutherford backscattering spectrum (solid curve) for as-deposited Co on GaAs. The dashed curve is the computer simulation of the spectrum. The individual contributions of Co, Ga, and As to the total simulated spectrum are also shown.

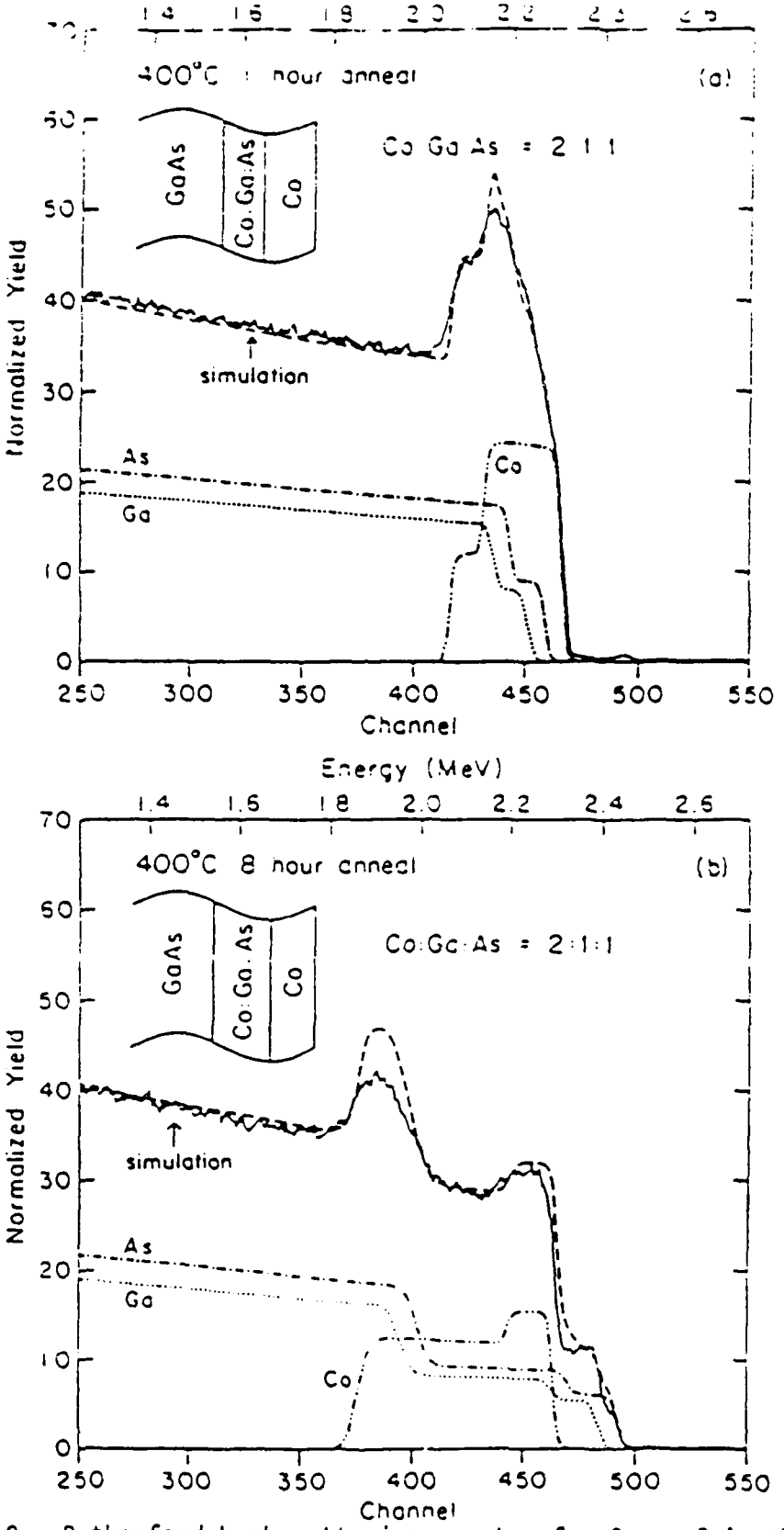

Figure 2. Rutherford backscattering spectra for Co on GaAs thermally annealed at 400°C for (a) 1 h and (b) 8 h. The dashed curve is the simulation of the spectrum, showing the reacted layer of composition Co:Ga:As = 2:1:1 between a layer of unreacted Co and the GaAs substrate. The individual contributions of Co, Ga, and As to the simulation are also shown. The step in the back edge of the Co contribution indicates partial reaction with the GaAs.

location of the step indicates that growth occurs at the cobalt/GaAs interface. The simulation shows that the reacted layer has an atomic ratio of Co:Ga:As = 2:1:1 with unreacted Co above it. Annealing for 8 h, Figure 2(b) results in a thicker reacted layer of the same composition, with unreacted Co still present. By 24 h, the layer had completely, with unreacted Co still present. By 24 h, the layer had completely reacted to the same composition ratio of Co:Ga:As (2:1:1).

Compound semiconductor/metal layers, such as GaAs/metal, have additional reaction possibilities not found in monoelement/metal systems (e.g., metal/Si). These include the possibility of forming a ternary phase and the possibility of phase separation into metal/Ga and metal/As phases. In the Ni/GaAs system, several groups have shown the existence of the ternary phase Ni_2GaAs at low temperatures [4]. At higher temperatures, the ternary decomposes into two binary alloys, NiAs and NiGa. Similar behavior was observed for Pd/GaAs, with a maximum temperature of 350°C for the ternary [9]. The backscattering data showed the composition of the cobalt/GaAs reacted layer to be that of Co:Ga:As = 2:1:1. However, RBS does not provide any information on the phase or phase forming that layer. Figure 3 shows the x-ray diffraction pattern obtained from the sample annealed at 400°C for 1 h. The dominant phase was indexed as the orthorhombic phase CoAs and showed strong preferred orientation. Weak lines from the simple cubic phase of CoGa were also present. A similar x-ray diffraction pattern was obtained from a sample annealed at 400°C for 4 h.

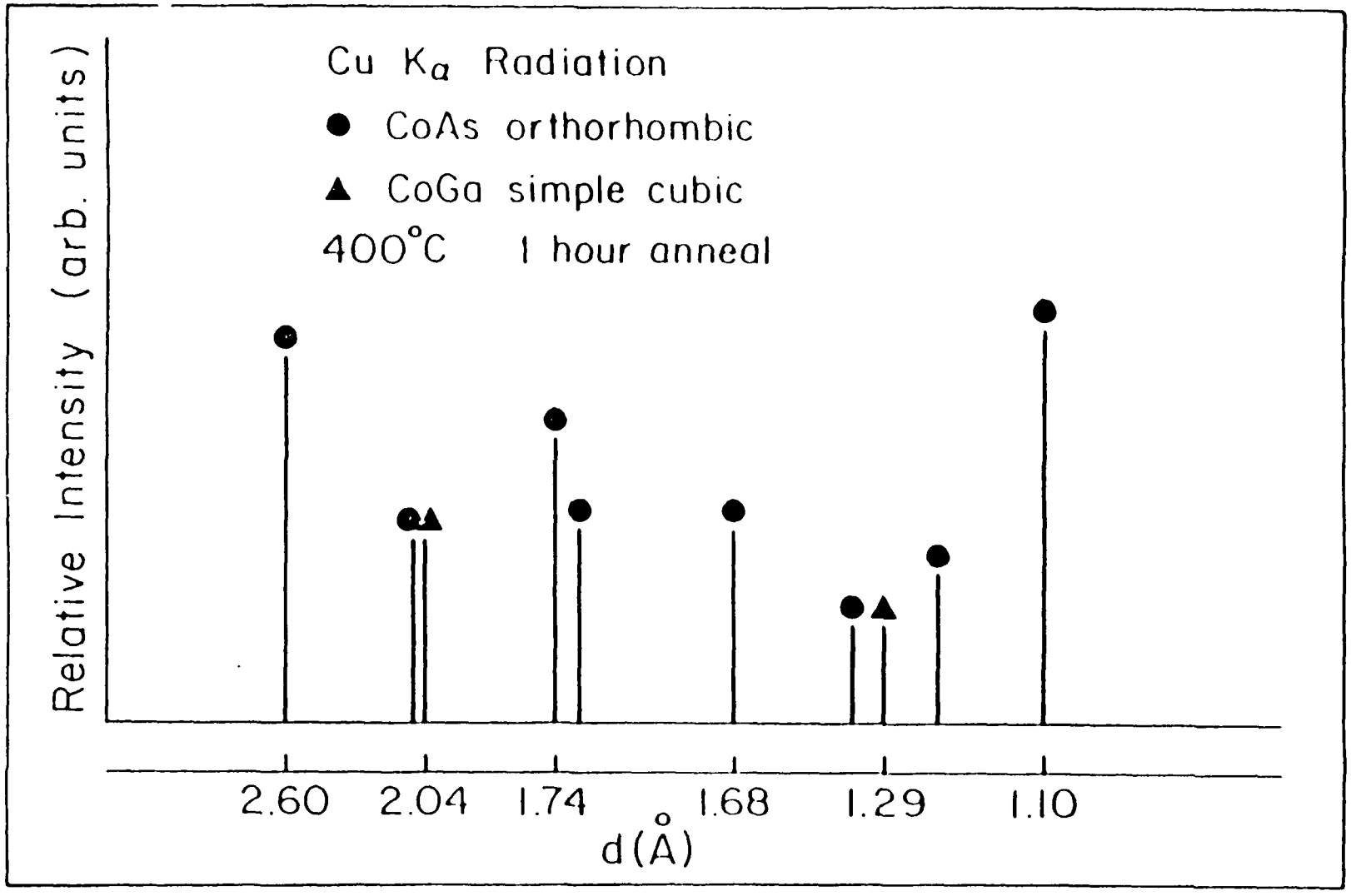

Figure 3. X-ray diffraction for reacted layer of composition Co:Ga:As = 2:1:1. The dominant phase can be indexed as orthorhombic CoAs.

Based on these results and the studies of Ni/GaAs and Pd/GaAs, we expect the reacted layer identified by RBS as Co:Ga:As = 2:1:1 to be a combination of CoGa and CoAs. However, this does not conclusively rule out the possibility of a ternary phase Co_2GaAs forming with a similar structure to CoAs. In the Ni/GaAs system for example, the phases NiAs and Ni_2GaAs are both hexagonal and have lattice parameters within 20% of each other [6].

The thickness of the reacted layer of composition Co:Ga:As = 2:1:1 (400^oC) is plotted in Figure 4 as a function of the square root of the anneal time. The ordinate of the plot shows thickness in terms of the anneal density (atoms/cm^2), which is what RBS actually measures. To convert atoms/cm^2 to the actual thickness requires knowing the density of the reacted materials. A least-squares fit to the thickness data is shown as the straight line in Figure 4. From the good agreement between the data and a linear dependence on the square root of time, one can conclude that the reaction is following diffusion controlled growth.

In conclusions, Rutherford backscattering analysis has been used to study thermally induced phase formation in the Co/GaAs thin-film system. Computer simulations have been shown to be beneficial, if not required, for the analysis of complex overlapping RBS spectra encountered in many metal/GaAs systems. At 400^oC, a reacted layer of composition Co:Ga:As = 2:1:1 is formed. The thickness of this layer increases with the square root of time until all of the metal is consumed. X-ray diffraction results indicate the dominant phase to have the structure of CoAs. The cobalt/GaAs

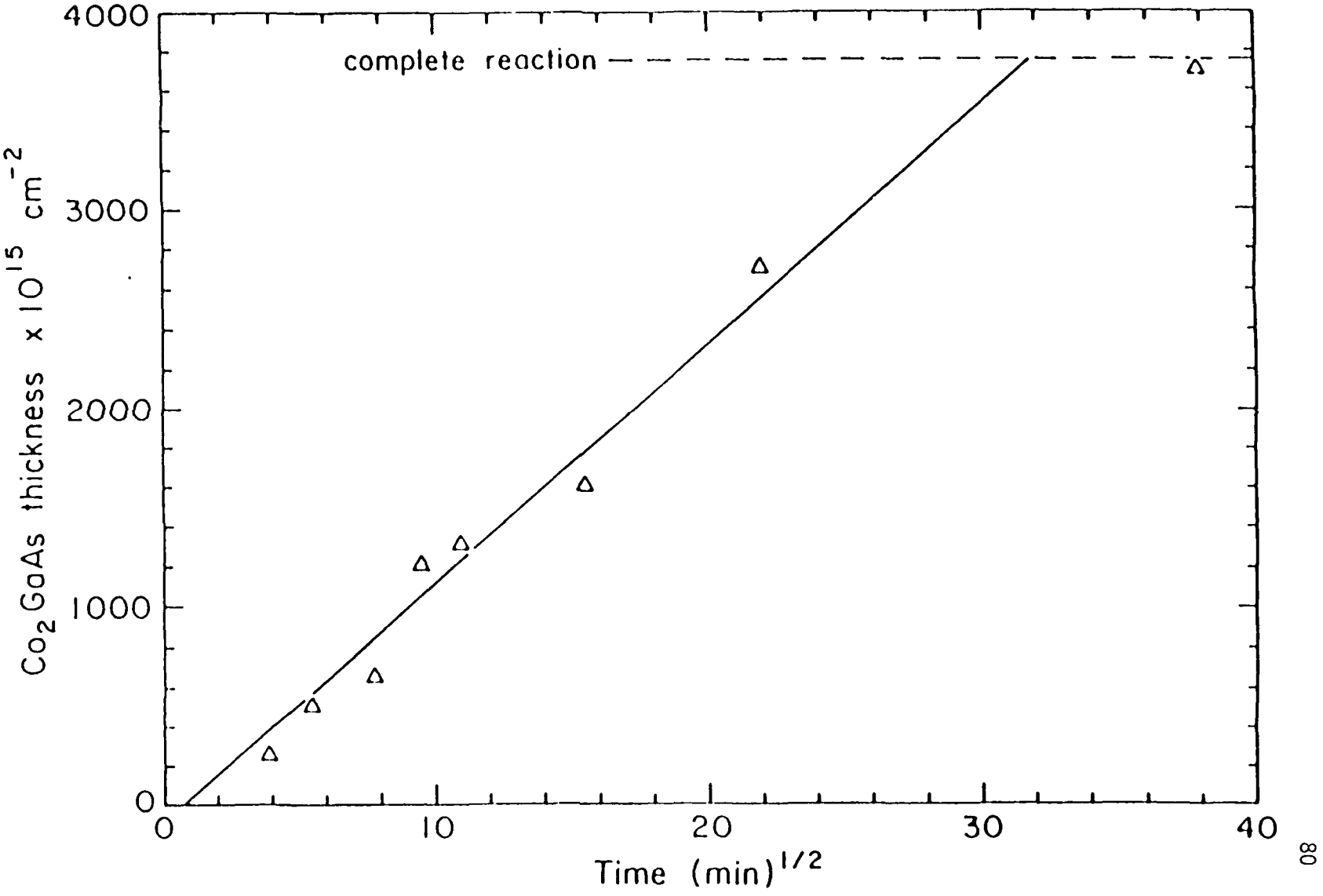

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Figure 4. Plot of the thickness of reacted layer of composition Co:Ga:As = 2:1:1 as a function of the square root of anneal time at 400°C. The dashed line marking the point of complete reaction was calculated based on the amount of deposited metal. The solid line is a least-squares fit to the data points.

system has exhibited controllable layer-by-layer growth analogous to metal/Si silicide forming systems. The results presented here are the initial stages of developing a systematic understanding of metal/GaAs thin-film reactions. Further studies are needed to determine phase formation and kinetics as a function of temperature, electrical properties, activation energies for growth, and microstructures of the reacted phases.

1. C.J. Palmstrom and D.V. Morgan, in Gallium Arsenide, edited by M.J. Howes and D.V. Morgan (Wiley, NY, 1985), Chap. 2.

2. C. Fontaine, T. Okumura and K.N. Tu, J. Appl. Phys., 54, 1404 (1983).

3. P. Oelhafen, J.L. Freeouf, T.S. Kuan, T.N. Jackson and P.E. Batson, J. Vac. Sco., Technol., B1, 588 (1983).

4. M. Ogawa, Thin Solid Films, 70, 181 (1980).

5. T. Yoshie, C.L. Bauer and A.G. Milnes, Thin Solid Films, 111, 149 (1984).

6. A. Lahav, M. Eizenburg and Y. Komem, Mater. Res. Soc. Symp., Proc. 37 (1985).

7. V. Kumar, J. Phys. Chem. Solids, 36, 535 (1975).

8. L.R. Doolittle, Nucl. Instrum. Methods, B9, 344 (1985).

9. J.O. Olowolafe, P.S. Ho, H.J. Hovel, J.E. Lewis and J.M. Woodall, J. Appl. Phys., 50, 955 (1979).

2. Solid Phase Epitaxial Growth of Ge on GaAs

Heteroepitaxial layers of Ge on GaAs may be of importance not

only for ohmic contacts to GaAs but also for devices utilizing the properties of this junction; one example could be a photodetector. Detailed investigations have been made of epitaxial layers grown either by molecular beam epitaxy (MBE) or by vacuum deposition of Ge on heated GaAs substrates [1-5]. These techniques rely on cleaning the GaAs surfaces by heating the GaAs to about 575^{o}C to desorb the native oxides and carbides. Deposition of a single crystal epitaxial Ge film is then done with the GaAs substrate held at temperatures about 300-500^{o}C. These epitaxial Ge layers have been used to produce ohmic contacts with exceedingly low specific contact resistance (less than or equal to 1 x $10^{-7}\Omega cm^{2}$) [5]. However, these techniques are not easily adapted for selective area growth of Ge on GaAs.

Since solid phase epitaxial growth involves post deposition annealing, it is more compatible with selective area growth. The Ge may be deposited onto conventionally patterned wafers and 'lift off' after deposition can be used to remove the unwanted Ge. Subsequent annealing will result in epitaxy of the remaining deposited Ge. Amorphous Ge layers on single crystal Ge substrates formed by ion implantation can be readily regrown at temperatures greater than 300°C [6]. However, deposited amorphous Ge films on Ge do not show good epitaxy for anneals less than about 750°C [7]. This has been attributed to surface contamination (native oxide) of the Ge crystal, which inhibits intimate contact between the single crystal substrate and the deposited amorphous layer. Ion beam interface mixing of the deposited Ge/Ge interface for improved epitaxy at low temperatures supports this interpretation [8].

PdGe was used as a transport medium for solid phase epitaxial growth of Ge on GaAs using a Ge/Pd/GaAs starting structure [9]. Si has been grown epitaxially on GaP using solid phase epitaxy by depositing the Si on GaP sputter cleaned and in-situ annealed (to remove the surface damage) [10].

Recently solid phase epitaxy of Ge on GaAs without the use of a transport medium and in-situ annealing was reported [11]. The crystalline quality of the Ge epitaxial layer was good as far as ion channeling could determine. This paper discusses the quality of epitaxial Ge layers grown using this solid phase epitaxy technique. The layers are studied using RBS-channeling, TEM and SIMS analysis techniques.

Undoped semi-insulating or Si-doped n-type GaAs substrates were degreased using trichloroethylene, acetone and methanol, rinsed in DI-water, etched in a mixture of $NH_4OH:H_2O_2:H_2O$ (1:1:40 by volume) for 1 minute and rinsed in a mixture of $NH_4OH:H_2O$ (1:5 in volume proportions). The samples were kept in the rinsing solution until they were ready for loading in the evaporator (less than 5 min.). Immediately prior to loading, the samples were blown dry using N_2 and then loaded into a vacuum load lock. The depositions were made using e-beam evaporation in a UHV chamber with a base pressure equal to or less than 1×10^{-9}Torr. The Ge was deposited at about 10 Å/sec at a pressure about 6×10^{-8}Torr. Prior to the Ge deposition the GaAs surface was sputter cleaned using an Ar^+ ion beam at 3 keV incident at 70^o to the sample normal. Sputtering was stopped once there was no oxygen or carbon detectable by in-situ

Auger analysis (after a typical dose of about 5 x 10^{15} Ar^+ ions/cm^2). After the Ge deposition some samples had an additional thin layer of V deposited on top of the Ge to act as a cap. Annealing of the samples was done in a separate turbo molecular pumped vacuum annealing furnace operating at a pressure of equal to or less than 2 x 10^{-7}Torr.

RBS-channeling spectra for a 1500 Å Ge layer before and after annealing at 400°C are shown in Figure 1. The channeled spectrum of the unannealed sample clearly shows the lack of alignment of the as deposited films. Cross sectional TEM investigations showed that the unannealed GE layers were amorphous. After annealing at 400°C for 1 hr a significant decrease in the channeling yield is observed. The Ge layer has partially regrown. The large peak at high energy in the channeling spectrum corresponds to unaligned Ge near the surface of the sample. However, the low yield beneath this peak indicates good alignment at the Ge/GaAs interface. This suggests that the Ge grows layer by layer from the GaAs surface towards the surface of the Ge. Further annealing of the sample did not improve the alignment of the Ge. When a layer of V was used as a capping layer on the Ge, epitaxial growth of the complete Ge layer is observed. This can be seen from the channeling spectrum in Figure 2. Note that there is no alignment of the V capping layer. The improved epitaxial growth of the capped Ge layers is probably due to the uncapped Ge layers absorbing impurities, oxygen and carbon, from the air after deposition and prior to annealing. The V cap inhibits impurity incorporation into the Ge layer. Figure 3 shows dark field

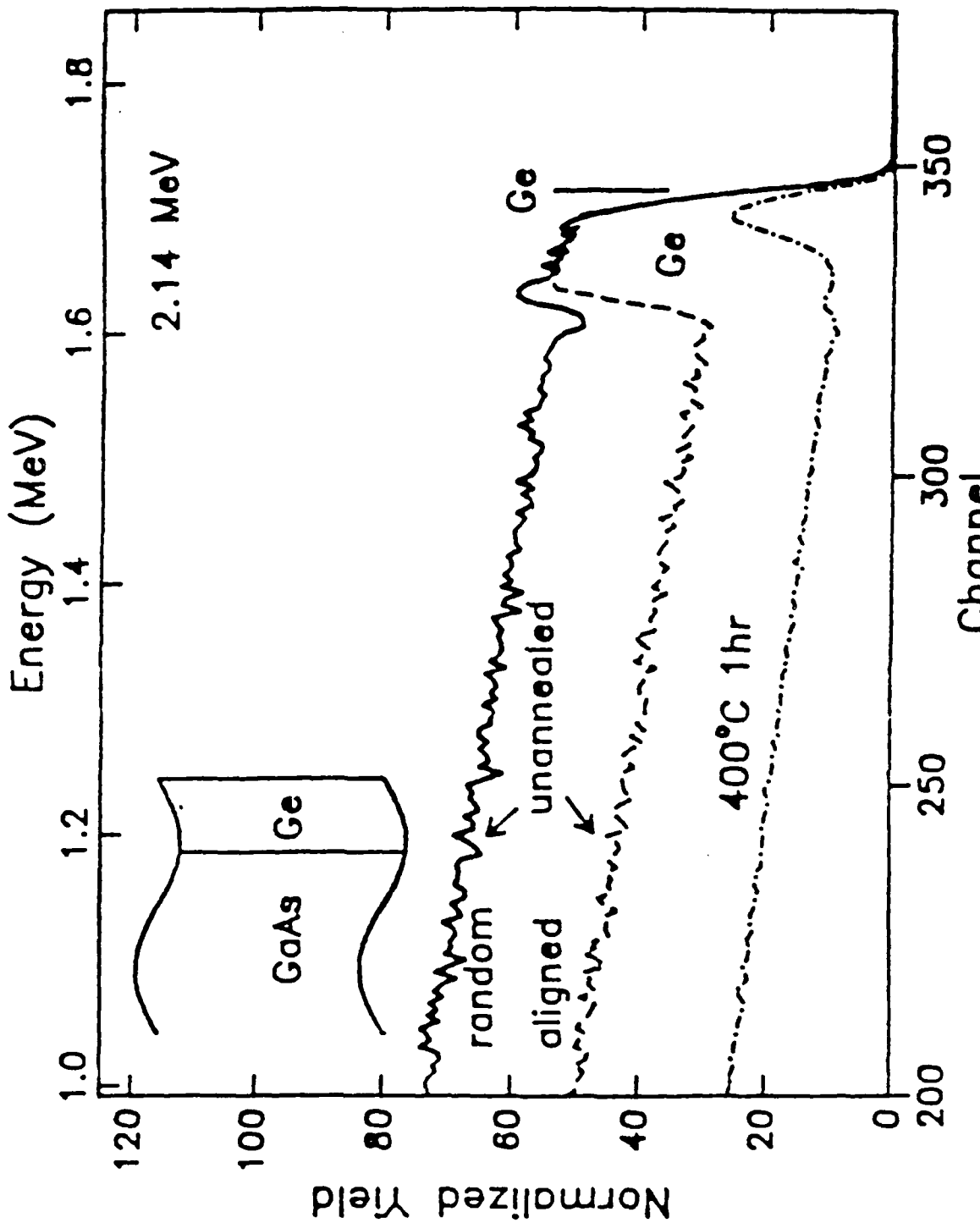

Figure 1. Backscattering channeling spectra of unannealed and 400°C 1 h annealed Ge (1500 Å)/GaAs structures.

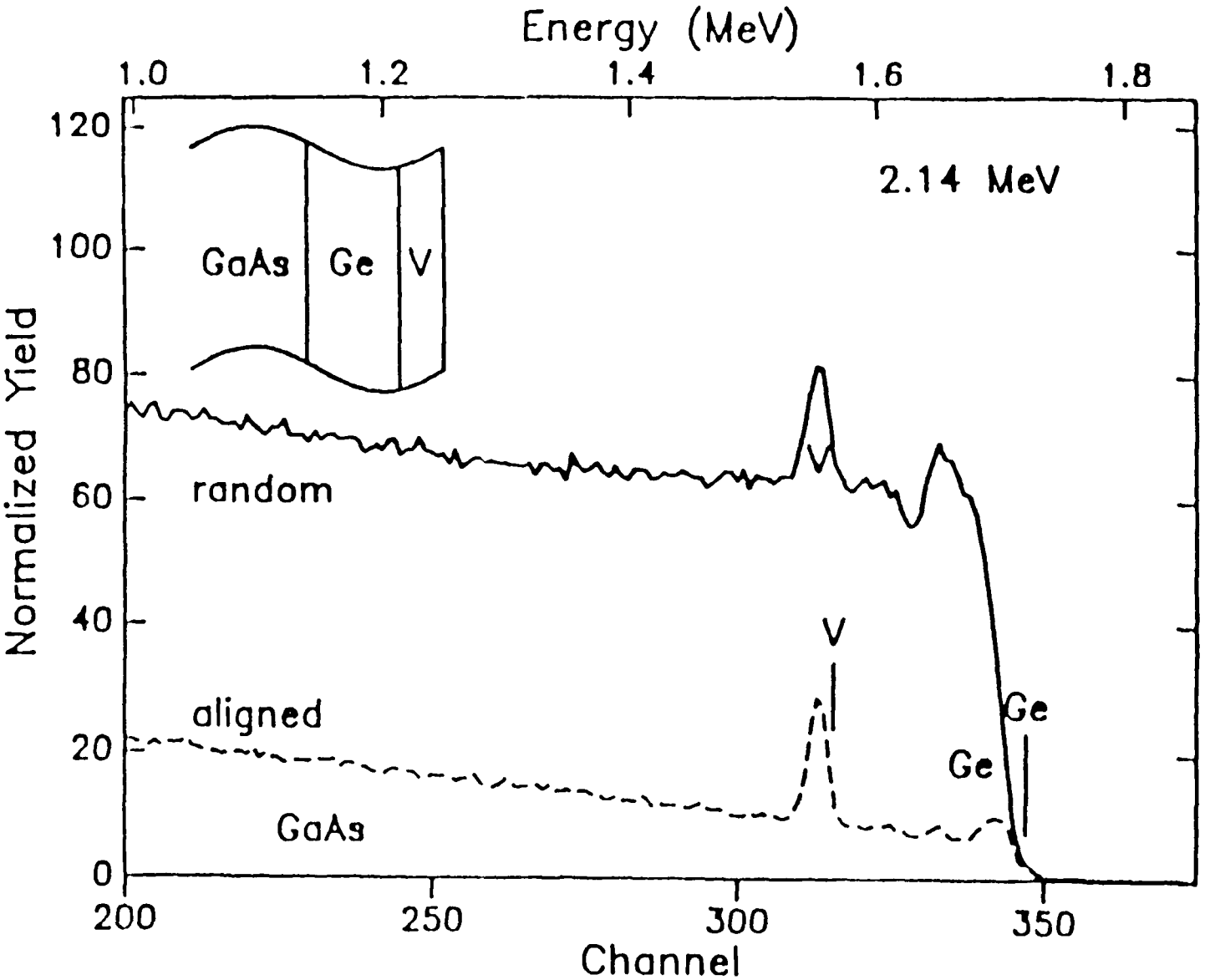

Figure 2. Backscattering channeling spectra of a 400°C 1 h annealed V(about 100 Å)/Ge (about 1000 Å)/ GaAs structure.

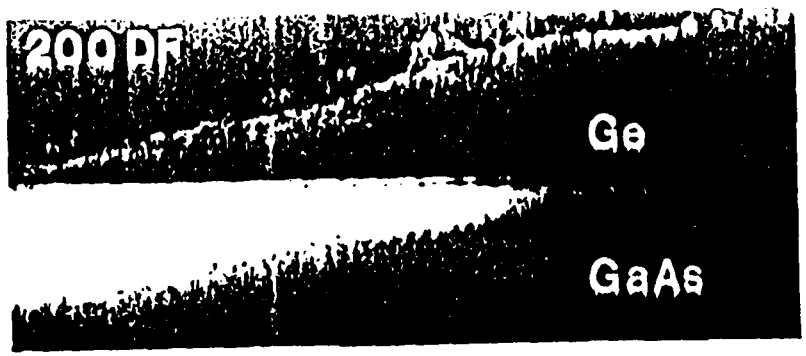

Figure 3. Dark field TEM cross sectional micrographs of an 400°C 1 h annealed V(about 200 Å)/ Ge(about 3000 Å)/GaAs structure.

cross sectional TEM micrograph of a V/Ge/GaAs sample which had been annealed at 400°C for 1 hr. The micrograph shows the edge of the hole formed during ion thinning of the specimen and hence some Ge has been removed. The complete Ge layer (3000 Å thick) is single crystal without any observable defects. The Ge and GaAs can be seen clearly from the contrast in this micrograph. However, the micrograph shows that there are some defects in the GaAs just beneath the Ge/GaAs interface (the dark line parallel to the interface). These probably arise from defects formed in the GaAs as a result of the sputter cleaning. The channeling measurements of this sample (Figure 4) show a x_{min} ~28%. Note that this is obtained for a Ge film beneath about 200 Å V layer and, therefore, does not represent a true measure of the crystallinity of the Ge film due to scattering in the V layer. This explains why the alignment in this sample was not as good as for the thinner Ge layers with thinner V capping layers (x_{min} ~10%). The surface As peak observed in the spectra in Figure 4 probably arises from As incorporation from the residual contamination in the annealing furnace rather than As outdiffusion through the Ge layer.

SIMS profiles of unannealed and 400°C 2 hr annealed Ge/GaAs structures are shown in Figure 5. The Ge/GaAs interface remains abrupt after the anneal. The concentration of Ge in the Ge film clearly increases during the anneal, indicating Ga outdiffusion. However, the Ga concentration in the Ge does not appear to be higher than that observed in MBE grown Ge/GaAs structures.

Since the concentration of Ga in the Ge layer is about the same as that observed for MBE grown Ge on GaAs, solid phase epitaxial

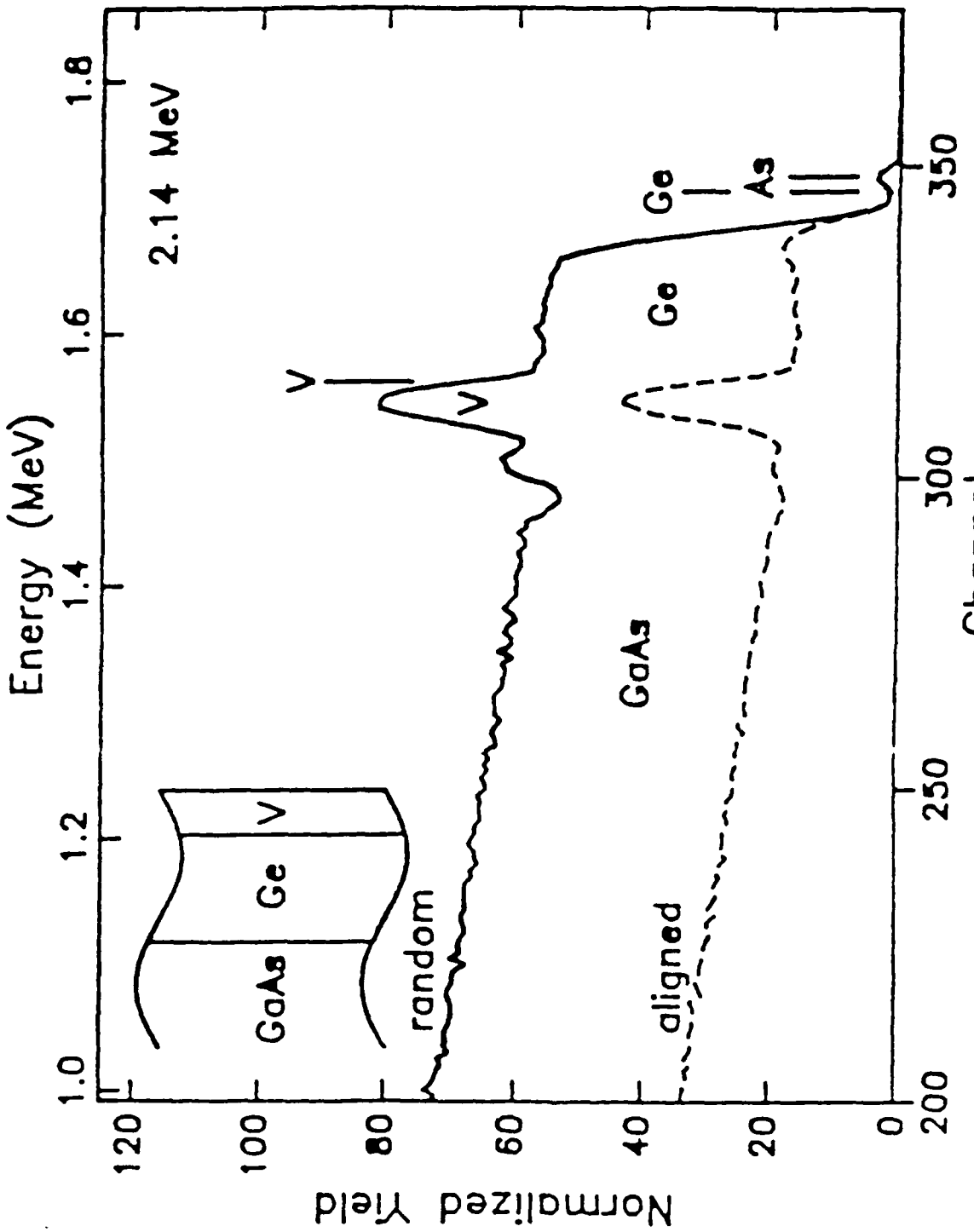

Figure 4. Backscattering channeling spectra of a 400°C 1 h annealed V(about 200 Å)/Ge(about 3000 Å)/GaAs structure.

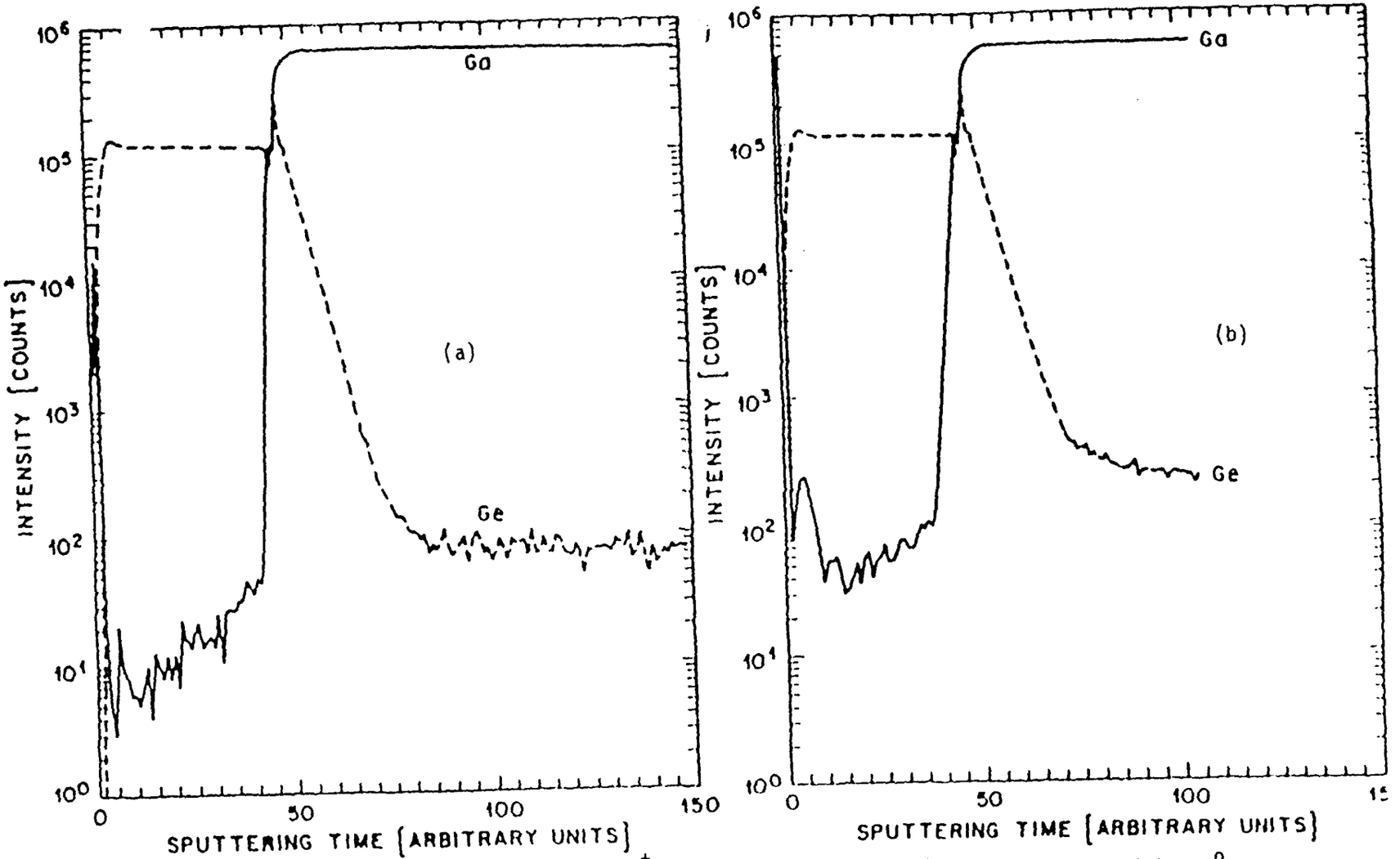

Figure 5. SIMS sputter depth profiles using O^+ sputteringf ions of: (a)unannealed and (b) 400°C 2 h annealed Ge (about 1500 Å)/GaAs structures.

growth of Ge on GaAs may potentially be used to produce device quality Ge. However, the major problem will not be the epitaxial growth itself but good control of the Ge/GaAs interface. The fact that the GaAs surface is sputter cleaned prior to Ge deposition poses two problems: a) damage of the surface GaAs, and b) possible preferential sputtering resulting in a nonstoichiometric GaAs surface. The first problem must clearly occur. However, if the damaged layer is thin enough, less than 200-400 Å, then the GaAs may be regrown by solid phase epitaxy during a subsequent anneal at equal to or greater than 250°C [12]. Since solid phase epitaxy of Ge is observed, this must be occurring. The technique described here relies on the fact that amorphous GaAs on single crystal GaAs starts to grow at equal to or less than 250°C and the Ge to grow at equal to or greater than 300°C. Hence, the GaAs surface regrows prior to the crystallization of the Ge and it then can act as a template. If this were not the case the Ge layer would be polycrystalline. Detailed studies of sputtering of GaAs surfaces will throw light onto the conditions required for stoichiometric surface preparation [13]. However, this nonstoichiometric surface could be used to tailor the interface properties by varying the degree of nonstoichiometry. The fact that complete solid phase epitaxial growth of 3000 Å of Ge is achieved for a 400°C 1 hr anneal suggests that the Ge/GaAs interface and Ge layer itself are clean.

Ge epitaxial layers have been grown on GaAs without the use of a transport medium or in-situ annealing prior to Ge deposition. The low annealing temperatures required for solid phase epitaxial

growth indicates that the Ge films and the Ge/GaAs interface are clean. The crystal quality is good as determined both by ion channeling measurements and cross sectional TEM investigations. The Ga outdiffusion into the Ge layer during solid phase epitaxy does not result in higher concentrations than when the Ge films are grown by MBE. This indicates that intentional doping of the Ge film should be possible.

1. R. Stall, C.E.C. Wood, K. Board and L.F. Eastman, Electron. Lett., 15, 800 (1979).

2. W.J. Devlin, C.E.C. Wood, R. Stall and L.F. Eastman, Solid-State Electronics, 23, 823 (1980).

3. W.T. Anderson, A. Christou and J.E. Davey, J. Appl. Phys., 49, 2998 (1978).

4. W.F. Tseng, J.E. Davey, A. Christou and B.R. Wilkens, Appl. Phys. Lett., 36, 435 (1980).

5. R.A. Stall, C.E.C. Wood, K. Board, N. Dandekar, L.F. Eastman and J. Devlin, J. Appl. Phys., 52, 4062 (1981).

6. L. Csepregi, R.P. Kullen and J.W. Mayer, Solid State Communications, 21, 1019 (1977).

7. M.G. Grimaldi, M. Maenpaa, B.M. Pine, M.-A. Nicolet, S.S. Lau and W.F. Tseng, J. Appl. Phys., 52, 1351 (1981).

8. C.J. Palmstrom, presented at 9th Symp. on Ion Sources and Ion-Assisted Technology (Tokyo, 1985).

9. E.D. Marshall, C.S. Wu, D.M. Scott, S.S. Lau and T.F. Kuech, in Thin Films and Interfaces II, edited by J.E.E. Baglin, D.R. Campbell and W.K. Chu (North Holland, New York, 1984), p. 63.

10. T. de Jong, F.W. Saris, Y. Tamminga and J. Haisma, Appl. Phys.

Lett., 44, 445 (1984).

11. C.J. Palmstrom and G.J. Galvin, Appl. Phys. Lett., 47, 815 (1985).

12. J.S. Williams and M.W. Austin, Appl. Phys. Lett., 36, 994 (1980).

13. Y.-K. Wang and P.H. Holloway, J. Vac. Sci. Technol., B2, 613 (1984).